DIODE APPLICATION HANDBOOK

FUNDAMENTALS, CHARACTERISTICS, APPLICATIONS

Design Engineer's Guide

nexperia

Diode Application Handbook

Fundamentals, Characteristics, Applications

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Preface

Welcome to the Nexperia *Diode Applications Handbook*. Like all of our other Design Engineer's Guides, the Diode Handbook is intended to be a practical, comprehensive and up-to-date reference work written by engineers for engineers, sharing expertise, application insights and best practice to help designers optimize their electronic circuits.

Nexperia and diodes share a common history dating back for the whole of the commercialisation of electronics. Diodes were – of course – one of the fundamental electronic components, first developed over 100 years ago. Similarly, Nexperia can trace its history back over 100 years with names like Mullard, Philips, Valvo, Signetics and NXP ringing through its lineage. Today, Nexperia's extensive portfolio includes diodes, bipolar transistors, ESD protection devices, MOSFETs, GaN FETs and analog & logic ICs, totaling more than 15.000 parts. Virtually every electronic design in the world uses Nexperia components, and these products are recognized as benchmarks in efficiency – in process, size, power and performance. 250 million parts are shipped every single day.

Despite being first developed in the early years of last century, diodes continue to play a vital part in electronic circuits. But, of course they have evolved beyond all recognition from the days of pioneers like Walter Schottky. Most recently, of course we have seen new materials such as silicon carbide emerge which are enabling the realization environmentally-responsible electric vehicles with the performance and range demanded by customers.

The goal of this new handbook – or to give it its full name – *Diode Application Handbook – Fundamentals, Characteristics, Applications: Design Engineer's Guide* is to be recognized as the technical dictionary for semiconductor diodes, sharing technical and application insights between the engineering community. Therefore, we proudly invite you to study our Diode Application Handbook – the table of contents will make it easy to navigate.

Finally, I would like to thank Dr.-Ing. Reza Behtash, who has significantly contributed to this edition.

Olaf Vogt
Director Product Application Engineering
Nexperia

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Chapter 1

Introduction

The history of semiconductor diodes underpins the entire history of electronics, and while it is easy to overlook diodes, today they have never been more relevant or diverse. Nexperia's diode expertise stretches back to the 1950s and the Valvo/ Philips Semiconductors facilities in Hamburg, Germany. In the intervening 70 years the company has built a very broad portfolio of devices including Small Signal Switching and Zener Diodes, very efficient Schottky Diodes and Power Rectifiers in modern Trench technologies.

Highlighting a few important milestones:

The development of special diodes with variable junction capacity, so called "Vericap" diodes, begins in 1964.

In the 1970s the production of Glass Diodes in the famous SOD68 commences. Nexperia is still known as the packaging innovator – the famous SOT23 3-pin package, invented in 1969, is still the world's largest-selling semiconductor package. In the 1980s and 1990s the number of 'leaded SMD' massively increased due to high-volume consumer products like PCs, Laptops, TVs etc. In the early 2000 diodes in leadless packages were introduced, supporting the needs of the record-breaking Mobile / Smart Phone Industry. Latest packaging considerations are discussed in Chapter 5 of this handbook.

The first decade of the 21st century was also when Nexperia built its successful ESD Diode product portfolio (readers are advised to read the ESD Application Handbook and the ESD Automotive Edition.)

Developments continue apace and in this current decade, there have been, perhaps for some, surprising introductions. How familiar, for example, are most readers with new silicon germanium products (the first SiGe rectifiers were brought to market in 2020 by Nexperia)? Another case in point is silicon carbide. A visit to a trade show or quick web search will confirm that SiC outperforms silicon devices in certain applications. But what are the material properties that deliver this performance boost and how can designers benefit most from new SiC rectifiers? This book will tell you.

The content of the Diode Application Handbook will benefit readers by sharing a wealth of technical information, from basic fundamentals up to design ideas.

Chapter 2 explains the fundamentals, looking at diode types and behavior. Chapter 3 looks at the parameters commonly listed in diode datasheets, and how to interpret that information. Chapter 4 is devoted to thermal considerations, and Chapter 5 focuses on one of Nexperia's key strengths: packaging innovation, which is so influential on reliability and performance. Chapter 6 concerns itself with reliability, including Automotive-grade qualification. The application's chapter (7) at the end of the handbook highlights several basic functions (including polarity

protection and freewheeling functionality for inductive loads) that diodes provide in electronic systems. These sub-circuit insights help to address real-world challenges in electronic design.

Earlier, we mentioned electric vehicles as one obvious example of an application where new diode technologies are playing a vital, enabling role: in reality, very few electronic systems exist without some form of diode performing a vital function. Diodes are used in data centers, 5G, robotics, IoT systems, 'smart' installations – home/office/factory/city – medical equipment, in consumer electronics like mobile phones and in high-reliability mission-critical space expiration.

Efficiency is the mantra of our times, either for reasons of size, power consumption, performance or cost, or perhaps all four. Correct component selection will optimize the final design; poor choices will lead to compromise. As one of the most fundamental electronics building blocks, the diode is – as readers will see – not merely the humble discrete component that can be considered at the last minute.

The Diode Applications Handbook will satisfy engineers who wish to get more insights on fundamentals and applications insights. The focus on engineering aspects and technical challenges provides vital background information that will enable the engineer to optimize designs to ensure best product performance. But the book never falls into the trap of becoming a mere academic exercise. Its pages detail practical solutions to real world problems with applicable circuits and formulas. Chapter 7, Diode applications and use cases, is particularly strong here with sections on polarity protection, ORing, hard switching, power supply design and more.

This reference work represents the collected knowledge of some of our industry's most respected experts. But these are people who deal on a daily basis with questions from engineers. They know what questions are commonly asked and they are delighted to be able to share their research and experience widely and freely. We hope that you find this work informative and useful.

Nexperia continually updates product information and application notes. Please visit our Nexperia Encyclopaedia handbook series *www.nexperia.com/design-engineers-guides* to read our other handbooks:

- MOSFET & GaN FET Application Handbook
- LOGIC Application Handbook
- ESD Application Handbook and
- ESD Application Handbook: Automotive Edition

Chapter 2

Diode fundamentals

2.1 Different types of diodes

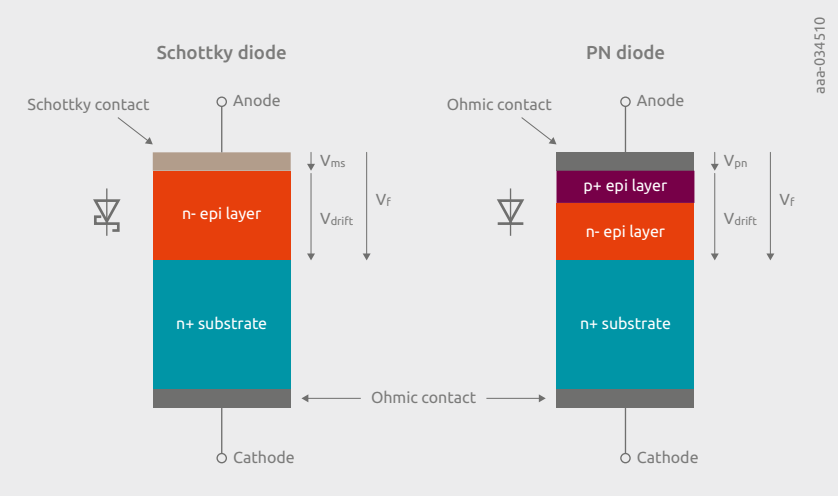


Figure 1 | Sketch showing the layer structure of Schottky (left) and PN diodes.

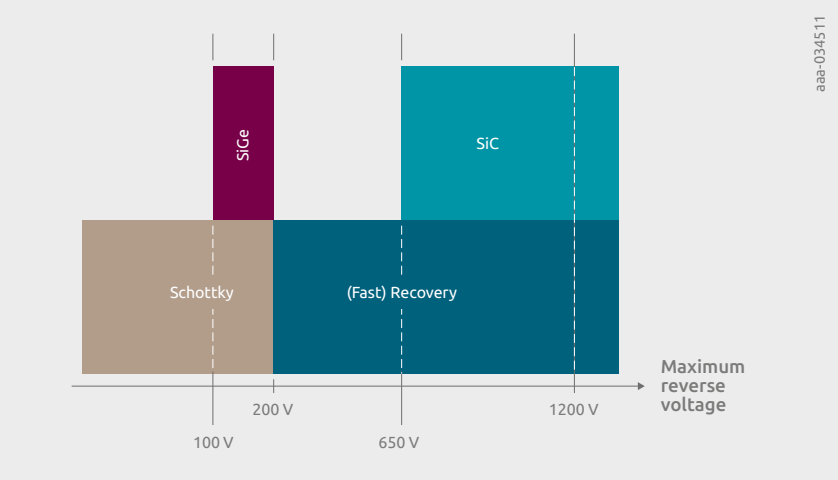


Figure 2 | Overview of different technologies for discrete diodes depending of max. reverse voltage.

An ideal diode will generally have a low forward voltage drop, a high reverse blocking voltage, zero leakage current and a low parasitic capacitance, facilitating a high switching speed. When considering the forward voltage drop, there are two main elements contributing to the overall voltage drop V_F, as shown in Figure 1: the voltage drop across the junction – a p-n junction in case of recovery rectifiers and Zener diodes and a metal-semiconductor junction in case of Schottky rectifiers; and the voltage drop across the drift region. The forward voltage drop across the p-n junction is intrinsically determined by the built-in voltage and hence, mainly by the chosen semiconductor and its doping. On the other hand, the forward voltage drop across the metal-semiconductor interface in a Schottky barrier rectifier can be modified by the choice of the Schottky metal, with the Schottky barrier being the result of the difference between the metal work function and the electron affinity of the semiconductor. By using Schottky metals with a low metal work function, the voltage drop across the metal semiconductor interface can be minimized. However, there is a trade-off between the forward voltage drop across the junction and the leakage current of the Schottky rectifier, as the level of the leakage current is also determined by the Schottky barrier and the electrical field across the metal semiconductor interface. In addition to this trade-off, the advantage of a low voltage drop across the junction can disappear when the thickness of the drift region is increased in order to achieve a high reverse blocking voltage. This is the reason why the reverse blocking voltage of Schottky rectifiers is traditionally limited to well below 200V. These considerations lead to the overview of utilized technologies for discrete diodes based on maximum reverse voltage, as shown in Figure 2. As already mentioned, Schottky diodes are normally used up to a maximum reverse voltage of approx. 200V; beyond 200V, Schottky diodes lose their intrinsic advantage. After this point, recovery rectifiers are used. A distinction is made for recovery rectifiers between different switching speeds. This classification will be described in the chapter on dynamic behavior (2.4). The operating range of a silicon carbide (SiC) diode starts at 650V. Thanks to the wide bandgap of SiC this range extends to well above 1700V. Figure 2 also shows a new technology called silicon germanium (SiGe). The maximum reverse voltage range of SiGe diodes is between 100 and 200V, at around about the interface between Schottky diodes and recovery rectifiers.

This chapter will discuss the various diode types and technologies regarding their internal structure, static and dynamic behavior.

2.2 Structure and functional principle

2.2.1 Recovery rectifiers (P(I)N diodes)

Recovery rectifiers are based on a classical p-n junction in the device structure. An n-doped drift layer is epitaxially grown on the n+ substrate which serves as the cathode of the vertical device. The anode of the diode is realized by implanting and diffusing a p dopant into the epitaxial layer. The p diffusion step determines the profile of the p well, and it is therefore crucial for the breakdown voltage of the diode. The maximum reverse voltage of recovery rectifiers starts at around 200V and increases to approximately 1700V. Diodes at the higher end of the reverse voltage range consist of a p-i-n-junction rather than a p-n interface, as the almost undoped layer between the p and n region allows for a further expansion of the depletion layer while the device is reverse biased. A top metallization layer is used to create an ohmic contact to the anode of the diode.

The Scanning Electron Microscope (SEM) image in Figure 3 shows the cross section of a recovery rectifier. In order to highlight the different doping regions, the sample has been treated with a special etchant, making the doping interfaces clearly visible. In this picture one can see very clearly the shape of the p well at the edge of the active region. This shape decides the contour of the depletion region of the p-n junction when the diode is reverse biased, and together with the field plate it forms the termination area for this device. Proper edge termination of the active cell is important in order to avoid the crowding of the electrical field in this area which could lead to premature breakdown and increased leakage current. Figure 4 illustrates a simplified sketch showing the contour of the depletion region and the resulting crowding of the electrical field at the edge of the active cell. As we will see later on, the termination design can also impact the dynamic behavior of the device. The epitaxial layer of recovery rectifiers is often intentionally contaminated with gold or platinum. The Au and Pt atoms in the silicon layers act as traps for the charge carriers and reduce the lifetime of minority carriers. This so-called 'lifetime kill' has a huge impact on the dynamic behavior of the device and will be discussed in section 2.4.

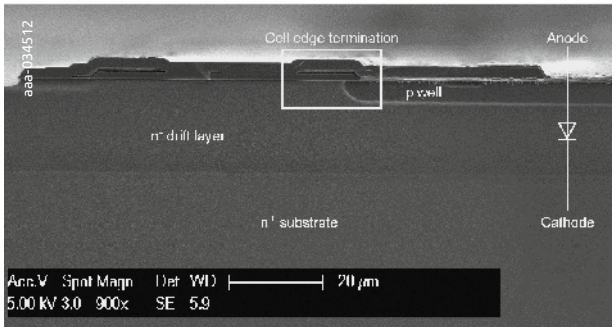


Figure 3 | SEM picture showing the cross section of a recovery rectifier. The sample has been etched in order to decorate the different doping regions.

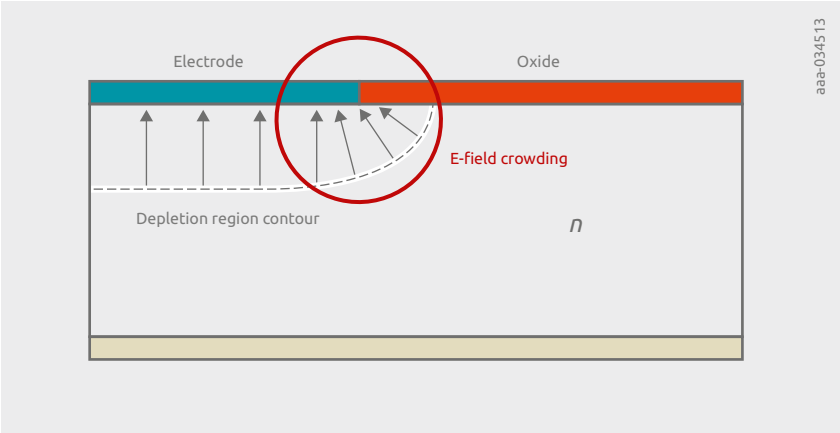


Figure 4 | The so-called 'E-Field crowding' at the edge of the active cell leads to premature breakdown and increased leakage current. A proper edge termination prevents the increased electrical field concentration at the edge of the active cell.

2.2.2 Planar Schottky diode

The Schottky diode – named after its inventor, the German physicist Walter Hans Schottky – consists essentially of a metal-semiconductor interface. Because of its low forward voltage drop and high switching speed, the Schottky diode is widely used in a variety of applications, such as the boost and buck diode in power conversion circuits. The electrical performance of a Schottky diode is, of course, subject to physical trade-offs, primarily between the forward voltage drop, the leakage current and the reverse blocking voltage. The most important consideration for balancing the trade-off between the forward voltage drop and the leakage current is the chosen Schottky metal. The higher the metal work

function of the Schottky metal, the higher the barrier height, and therefore the higher the forward voltage drop and the lower the leakage current of the Schottky diode (and vice versa). The breakdown voltage of the Schottky diode on the other hand is primarily determined by the choice of the epitaxial layer thickness and doping.

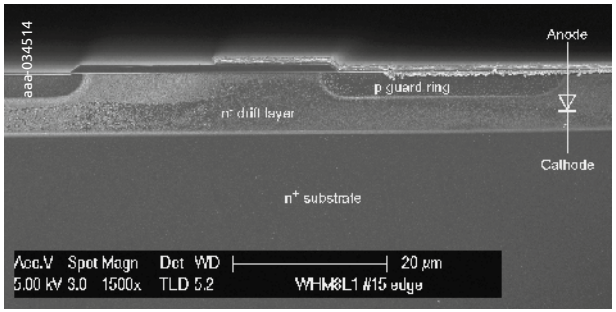


Figure 5 | SEM picture showing the cross section of a planar Schottky diode. The sample has been etched in order to highlight the different doping regions. The termination consisting of guard ring and field plate is clearly visible.

Figure 5 illustrates the cross section of a planar Schottky diode. The sample has been etched in order to delineate the different doping regions in the device. The etching also highlights the edge termination concept of the planar Schottky diode. The so-called 'guard ring' consists of a p-doped region beneath the oxide opening at the edge of the active area. The guard ring has a huge impact on the leakage current of the Schottky diode as it prevents the electrical field crowding at the edge of the active region, as discussed earlier and shown in Figure 4. But the guard ring is also ultimately a pn junction at the edge of the active area parallel to the actual metal-semiconductor junction. When the diode is forward biased with a high forward voltage – high enough to switch on this pn diode, the guard ring contributes to the forward current of the Schottky diode, enhancing the current capability of the device. But it can also have a detrimental effect on the switching behavior of the Schottky, as will be discussed later in the dynamic behavior section 2.4.

2.2.3 Trench Schottky diode

The widely-known one-dimensional silicon limit describes the general trade-off between the achievable breakdown voltage and the specific on-resistance of a silicon layer sandwiched between two electrodes. One could overcome the 1D silicon limit and decrease the specific on-resistance for a given breakdown voltage by flattening the profile of the electrical field in the semiconductor layer. In an ideal case, the electrical field would be constant along the drift layer rather than having a peak surpassing the critical electrical field in the given semiconductor. There are basically two concepts for flattening the electrical field profile which are used in commercial products: the super junction and the trench. The concept behind the

Trench Schottky rectifier is termed 'RESURF' (reduced surface field). The RESURF effect is illustrated in Figure 6. In a planar Schottky rectifier the equipotential lines are concentrated close the top electrode, resulting in a high electrical field near the surface. This results in a strong increase of the leakage current with increasing reverse voltage, and an early breakdown when the critical electrical field is exceeded near the surface.

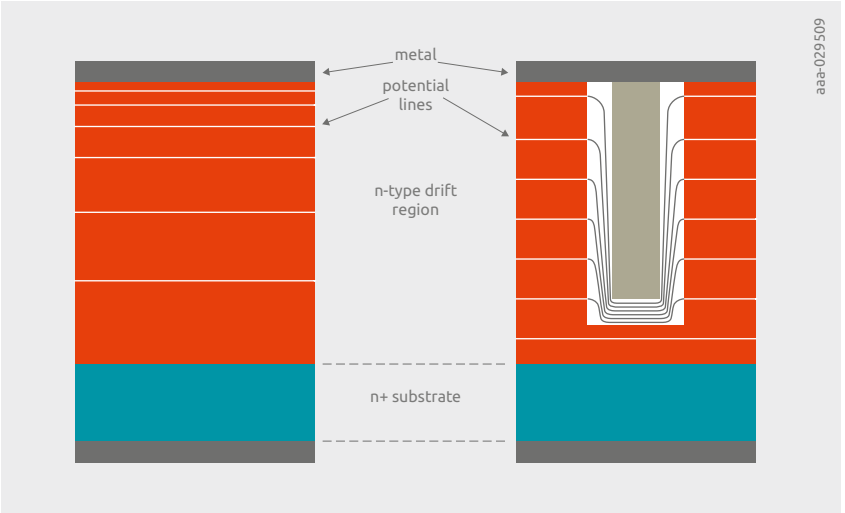


Figure 6 | Equipotential lines in a planar Schottky rectifier (left) and in a Trench Schottky rectifier (right) in reverse direction.
The top metal layer represents the anode, the bottom metal layer is the cathode.

By etching trenches into the silicon and filling them with polysilicon – electrically separated from the drift region by a thin dielectric – the trenches act like a field plate in the semiconductor, depleting the drift region in reverse direction and resulting in a flattened electrical field profile along the drift region. Therefore, the maximum electrical field is occurring inside the dielectric layer at the bottom of the trench rather than at the surface of the epi layer. The trench concept gives the device designer an additional degree of freedom to design and to optimize the device with respect to one of its parameters. Therefore, it is possible to use trenches to reduce the leakage current of the Schottky diode for a given epitaxial layer thickness, doping and Schottky metal. This is illustrated in Figure 7, where the reverse characteristics of a planar Schottky diode is compared to a Trench Schottky diode with the same epitaxial structure (doping and thickness), and the same Schottky metal and die size.

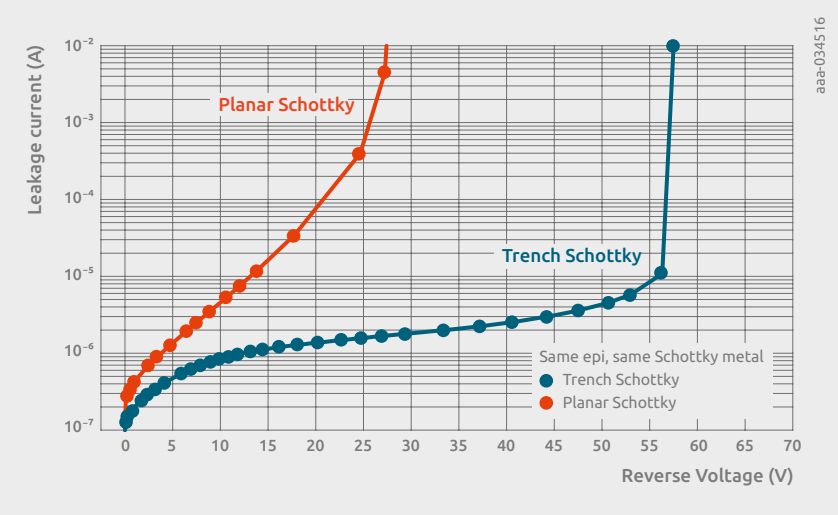


Figure 7 | The reverse characteristics of a planar Schottky vs. a Trench Schottky with the same epitaxial thickness and doping, same Schottky metal and die size.

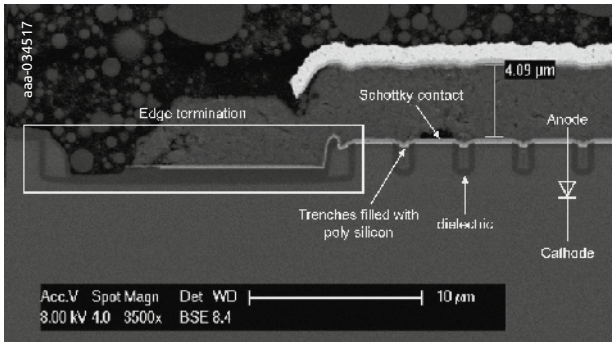


Figure 8 | SEM picture showing the cross section of a trench Schottky diode. The edge termination area is highlighted and consists of a wide trench covered by a field plate. Consequently there is no guard ring and thus no pn junction (as would occur for a planar Schottky).

However, it is also possible to use trench technology to improve the forward voltage drop V_F of the Schottky diode, by increasing the doping concentration of the epitaxial layer without sacrificing the leakage current level of the device. This can also be useful for a die-shrink to house the diode in a smaller package.

The cross section of a trench Schottky diode is shown in Figure 8. Aside from the trenches, an obvious difference to a planar Schottky design is the termination concept, which consists of a wide trench. A field plate covers this trench to its center. Consequently, there is no guard ring and thus no pn junction in the device, at least for trench Schottky diodes with a maximum reverse voltage of up to approximately 100V. The impact of this termination concept on the switching behavior of the Trench Schottky diode will be discussed in section 2.5.4.

2.2.4 Silicon germanium (SiGe) diode

Silicon germanium (SiGe) is a compound semiconductor well known as the base material for hetero-junction bipolar transistors (HBT) since the 1990s. Over the last years, Nexperia has adapted this Technology for use in diodes. At the beginning of 2020 the first SiGe rectifiers were brought to the market by Nexperia.

When considering performance, the SiGe diode can be interpreted as a hybrid technology between Schottky and a recovery rectifier (PN diode). It combines the high efficiency of Schottky rectifiers, in terms of a low forward voltage drop, with the low reverse leakage currents and the thermal stability of PN diodes.

To better comprehend the excellent trade-off between V_F and I_R Figure 9 shows the structure of the SiGe diode. The epitaxial layers of the devices are grown on standard n+ silicon substrates. Therefore, conventional tools and processes are used for mass production. On top of the n– drift layer there is a very thin and highly p-doped silicon germanium layer. One obstacle to overcome is the accurate formation of the SiGe interface, as the lattice mismatch between silicon and germanium is greater than 4%. To prevent the interface having misfit dislocations, investigations have shown that reliable junctions may be formed if the germanium content is low and the SiGe layer is thin. *[Ashburn, Peter (2003): SiGe Heterojunction Bipolar Transistors, University of Southampton, UK: John Wiley & Sons, Ltd]*. The cathode of the diode consists of the back side metallization which forms an ohmic contact, as with other diode types.

The thin SiGe layer leads to a big gradient of the electron concentration, as illustrated in Figure 9. Along with the higher intrinsic carrier concentration of SiGe compared to Si ($n^2_{i\,SiGe} >> n^2_{i\,Si}$ as a result of the smaller band gap), this leads to a significant diffusion component of the current in the structure: $J = q \times D_n \times \frac{\partial n}{\partial x}$. This means that for a given forward voltage drop, a higher current density can be achieved with this structure as compared to a pure p-n junction. Equally, if V_F is lower, there is less stored charge in the layer for a given current density. This also results in an improvement in the switching behavior of the SiGe diode as compared to recovery rectifiers, as will be shown in section 2.5.

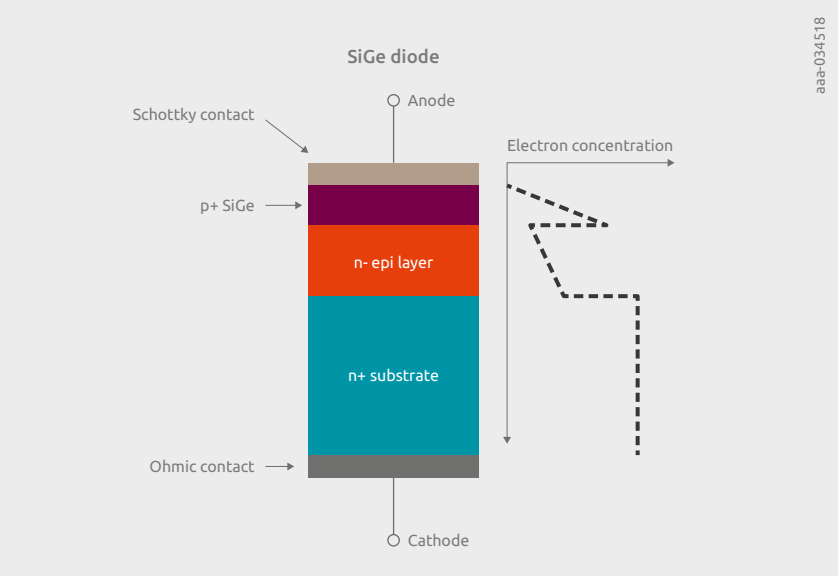


Figure 9 | Structure of the SiGe diode together with simplified electron concentration along the structure. The very thin and highly p-doped silicon germanium layer together with the higher intrinsic carrier concentration of SiGe (due to its narrower bandgap leading to ${n_i}^2_{SiGe} \gg {n_i}^2_{Si}$) leads to a significant diffusion current in the structure: $J = q \times D_n \times \frac{\partial n}{\partial x}$.

2.3 Static behavior

The static behavior of a diode is described by its current/voltage (IV) characteristics in forward and reverse direction in the data sheet. As an example, the IV characteristics of the Schottky diode PMEG045V150EPD are shown in Figure 10. Both the forward characteristics and the reverse characteristics exhibit a strong temperature dependence. The higher the temperature the lower the forward voltage drop, and the higher the leakage current of the diode in reverse direction. This is the case for all diode technologies, whether controlled by a metal semiconductor junction as in the case of Schottky diodes or a pn junction as for recovery rectifiers. In forward direction, the exponential dependence of the forward current on the forward voltage can be seen as a straight line on the logarithmic scale. As a general approximation, a voltage drift of approximately −1.7mV per Kelvin increase can be assumed for the impact of temperature on V_F (and approximately −2mV per Kelvin for recovery rectifiers). At higher currents, the impact of the voltage drop across the epitaxial layer increases and limits the current capability of the device. This leads to the observation that in this region, the curves for almost all temperatures run together. In reverse direction (right picture in Figure 10) there is also an exponential impact of the temperature on the reverse leakage current. Here, too, the exponential temperature dependence is not limited just to Schottky devices; it is also the case for recovery rectifiers. It is also interesting to mention that the different diode technologies share the fact that the breakdown mechanism in these devices is dominated by the avalanche breakdown.

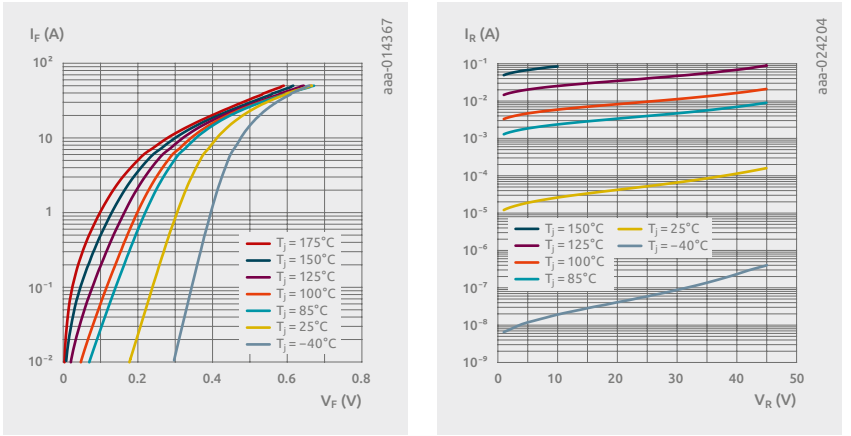


Figure 10 | IV characteristics of PMEG045V150EPD. Left: forward characteristics, right: reverse characteristics. Please note: all points are measured in pulsed mode, excluding any self-heating of the device.

In contrast to tunneling breakdown, the breakdown voltage caused by avalanche effect increases with temperature, as the rate of scattering mechanisms for the electrons increases with temperature, reducing the energy of the charge carriers and thus reducing the avalanche effect.

Now let us compare the static behavior of the different described diode technologies. Since the currents of the diodes in forward and reverse direction naturally scale with the size of the die (strictly speaking with the size of the active area), a normalization of the currents with respect to the die size is necessary in order to have a fair comparison of the different technologies. And as the different diode technologies are designed for different voltage ranges, it is also necessary to choose a voltage range that is reasonably suitable for all technologies. For this reason, Figure 11 shows the forward current density for several diode types used in the 100V voltage range. The diode technologies under investigation are: 120V silicon germanium, planar Schottky with a barrier height of 805meV, planar Schottky with a barrier height of 665meV, 200V hyper fast recovery rectifier (hyper fast recovery rectifiers are not available below 200V) and finally 100V Trench Schottky with a barrier height of 750meV. In this graph, the forward current is normalized with respect to the active area of the device. For Trench Schottky devices this means that the currents are normalized with respect to the sum of all mesa areas.

As expected, the forward voltage drop V_f is the highest for the hyper fast recovery rectifier for a given current density. The reason is obvious: the built-in voltage across the pn junction needs first to be equalized before a significant amount of current starts to flow. Thanks to the bipolar nature of the hyper fast recovery rectifier, these devices show a distinctive current-carrying capability up to high current densities.

The advantage of silicon germanium technology described in 2.2.4 can also be seen in Figure 11 as the SiGe diode exhibits significantly more current density for a given forward voltage compared to the hyperfast recovery rectifier. So, if the die size is limited by a specific type of package (and thus by the maximum die size in this package) it can be advantageous to use a SiGe die instead of a recovery diode in order to get more current out of the given package.

Now let's have a look at the unipolar devices in Figure 11. In a Schottky diode, the forward current is transported via thermionic emission. The majority carriers have to overcome the barrier height in order to transport the current. Therefore, the higher the barrier height the higher the necessary forward voltage for a given current density. This is the reason why the planar Schottky device with a barrier height of 805meV exhibits the highest forward voltage drop amongst the investigated Schottky diodes. The planar Schottky with a barrier height of 665meV has a low forward voltage drop for low current densities, however the curve

flattens out very quickly. This is due to the thick drift layer of this 100V device with such low barrier height, which is necessary to achieve the required breakdown voltage and to control the leakage current in reverse direction. This thick drift layer leads to a significant voltage drop across this layer at higher current densities, limiting the current transport capability of the diode. This is already described in section 2.1 which details why the reverse blocking voltage of Schottky diodes is limited to a voltage range of 150–200V. Otherwise very high barrier heights would be necessary for higher reverse voltages, which, in turn, would increase the forward voltage drop and diminish the current capability.

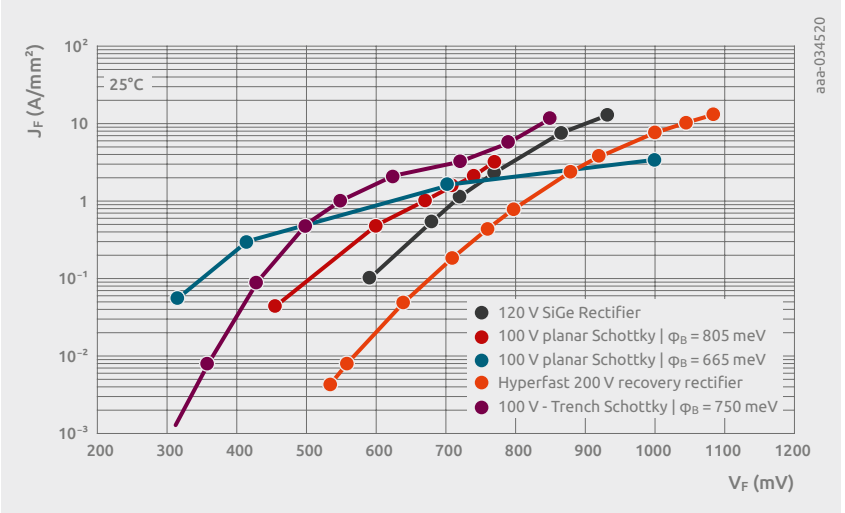


Figure 11 | Pulsed forward current density (normalized forward current with respect to the active area) for different 100V technologies at room temperature.

Section 2.2.3 describes that, because of the RESUR effect, Trench Schottky devices can have a significantly higher doping level in the drift layer compared to their planar counterparts, without suffering penalties regarding breakdown voltage or leakage current. This can be seen in Figure 11. The Trench Schottky device with a barrier height of 750meV has a higher forward voltage drop for low current densities compared to the planar Schottky with a barrier height of 665meV. However the curve doesn't flatten when the forward voltage is increased – as in case of the planar Schottky. This is due to the higher doping of the drift layer, resulting in significantly less voltage drop across the drift layer. The low-ohmic drift layer reveals yet another phenomena, the so-called 'hole-injection'. There are holes above the Fermi level in the Schottky metal which can be injected from the metal into the semiconductor (equivalent to valence band electrons in the semiconductor acquiring enough thermal energy to leave the silicon and enter into one of the

empty states above Fermi level in the metal, leaving behind a hole in the valence band). The barrier height for these holes entering the semiconductor is not high – just the difference between the band gap energy of silicon and the barrier height for the electrons. This, in turn, means that the hole injection is higher when the metal work function of the chosen Schottky metal is higher ('low leakage' Schottky metals have more hole injection).

In equilibrium or in low forward voltage bias, the injected holes are 'trapped' in a potential well below the valance band. But if the Schottky diode is under strong forward bias, the holes can leave the potential well and contribute to the current in the device. So, surprisingly, the unipolar Schottky diode can also have a bipolar component under strong forward bias, especially for high barrier types. This can be seen in Figure 11 for the Trench Schottky device at around 700mV forward bias. The whole injection can also be observed for the planar Schottky diode with the barrier height of 805meV at around 750mV, whereby it is less pronounced, as a higher forward voltage would be necessary in order to drive this device into strong forward bias.

The forward characteristics is Figure 11 were all measured at room temperature. At higher temperatures the curves will of course shift but the order and the discussed tendencies will remain intact.

Now let's consider the reverse characteristics of the same devices which were discussed in forward bias. Again, for this comparison of different technologies it is appropriate to normalize their reverse currents with respect to the active area of the die. However, a graphic of the leakage current density at all temperatures and all voltages fr all technologies would quickly become very confusing. For this reason we have concentrated on a fixed voltage and will discuss development of the leakage current density over the temperature range for a fixed voltage. A reverse bias voltage of –60V has been chosen for comparing the reverse characteristics of the different 100V technologies. –60V is high enough to reflect the blocking capability of the diodes but also low enough not to be affected by the incipient breakdown of the device.

The result is displayed in Figure 12. The hyper fast recovery rectifier, a device based on a pn junction, has a very low leakage level. The leakage current density increases approximately one order of magnitude for every 40°C increase in junction temperature. Interestingly, the leakage current density for the SiGe diode is even below the level of the recovery rectifier up to a junction temperature of 90°C. The rate at which the leakage current of the SiGe diode increases is steeper than for the hyper fast recovery rectifier. This is due the hybrid nature of the SiGe diode, also featuring a Schottky contact. Overall, the level of the leakage current density for the SiGe diode is very low, comparable to the hyper fast recovery rectifier. Together with the advantages already discussed over the hyper fast recovery rectifier in the

forward direction (see Figure 11), the value proposition of the SiGe diode becomes apparent. With regard to Schottky diodes, the influence of the electron barrier height as the determining factor can be seen quite clearly. As expected the planar Schottky device with the lowest barrier height (665meV) shows the highest leakage current density, which again illustrates the well-known trade-off between the forward voltage drop and the leakage current for Schottky diodes. The exponential dependence of the leakage current on the barrier height leads to a significantly reduced leakage current levels for the device with the barrier height of 805meV compared to the one with 665meV. In the case of the trench diode, despite the advantages in the forward direction, there are no disadvantages in the reverse bias. The leakage current is determined by the barrier height and the trench technology helps to control the course of the leakage current over the reverse voltage despite the high doping level in the epitaxial drift layer. (This is not shown in this graph, please refer to a Trench Schottky diode data sheet.)

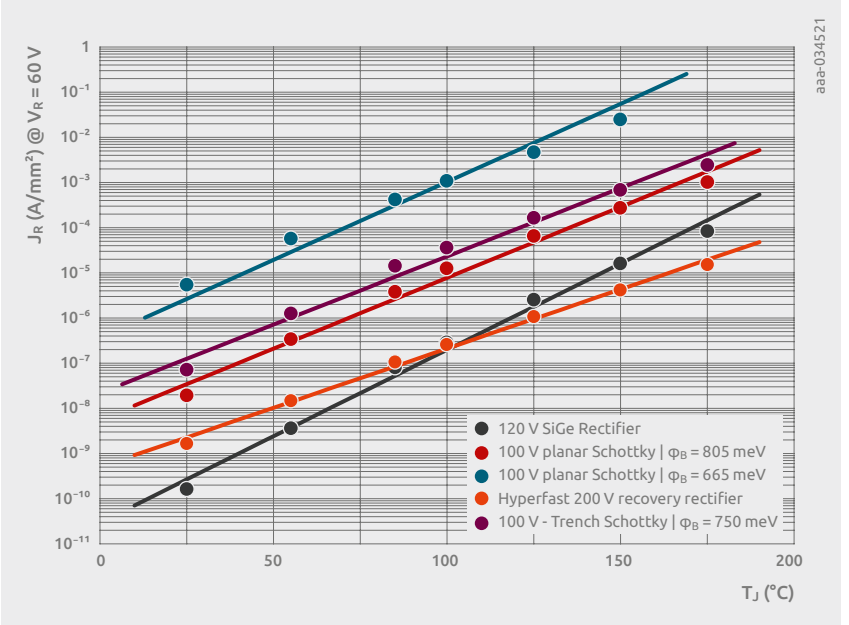


Figure 12 | Dependence of the leakage current density (normalized leakage current with respect to the active area) at a reverse bias voltage of –60V on the junction temperature for different 100V technologies.

2.4 Dynamic behavior

In many applications, a diode is not operated statically, but it is switched on and off continuously. The switching performance of the diode is critical for the efficiency of a system, such as, for example switched-mode converters.

2.4.1 Forward recovery

When a diode is switched on, it takes some time for the low-doped drift zone to become flooded with charge carriers. Thus, an increased initial forward voltage drop can be observed when the diode is switched on, because the drift zone does not yet have the necessary conductivity. This so-called forward recovery of the diode is characterized by the parameter V_{FRM} which describes the switch-on voltage peak and the forward recovery time t_{fr}. Depending on the thickness and doping of the drift layer, the forward recovery can be quite noticeable and must be considered during circuit design.

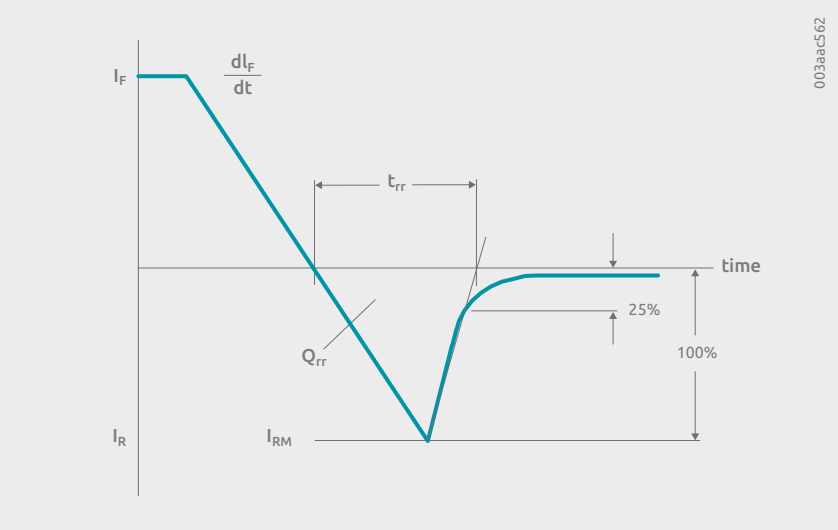
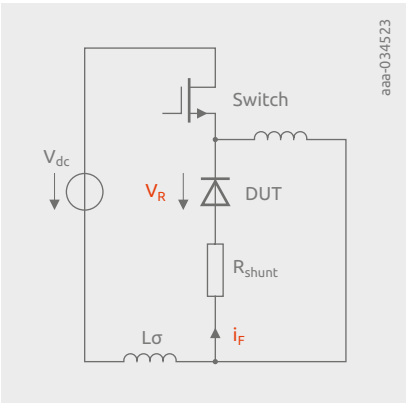


Figure 13 | The ramp reverse recovery definition for diodes.

2.4.2 Reverse recovery

Reverse recovery describes the dynamics with which the diode switches from the forward direction into the reverse blocking stage. When the diode is biased in the forward direction, the bulk material is flooded with charge carriers. If the polarity of the voltage across the diode is now reversed, it takes a finite amount of time until these excess charge carriers are removed. Only then can the space-charge region build up and the reverse voltage can be taken by the diode.

Figure 13 illustrates the defined parameters of the ramp reverse recovery. First, the diode is biased in forward direction, carrying the current I_F. It is obvious that the level of the forward current has a significant impact on the excess charge in the device and therefore on the dynamics of how fast the stored charge can be removed. This impact will be discussed later in detail. The rate di/dt defines how fast the forward current through the diode is switched off. Here, too, it is evident that a higher di/dt places higher demands on the switching performance of the diode. As shown in Figure 13, the current through the diode even passes the zero line and becomes negative. Notice that at this point that there is still excess charge in the device and no space-charge region has yet built up. The space-charge region starts to build up when the maximum reverse current I_{RM} is reached, and then it will take over the reverse voltage. The negative current starts to decrease while the reverse voltage across the diode starts to increase. Eventually the negative current through the device adjusts to the leakage current of the diode. The time between the point when the current crosses the zero line and becomes negative and the point in time when it reaches 25% of the maximum reverse current I_{RM} (this point being extrapolated linearly as shown is the graph – in some data sheets 10% is specified instead of 25%) is called reverse recovery time t_{rr}. The next important parameter is the stored charge Q_{rr} in the device which corresponds to the area below the horizontal zero line (the integral of the diode current within t_{rr}).



After defining the parameters of the ramp reverse recovery let's have a look how these parameters impacts the switching losses in a switched-mode converter.

Figure 14 | Double-pulse test: basic circuit used for characterizing the switching behavior of the diode.

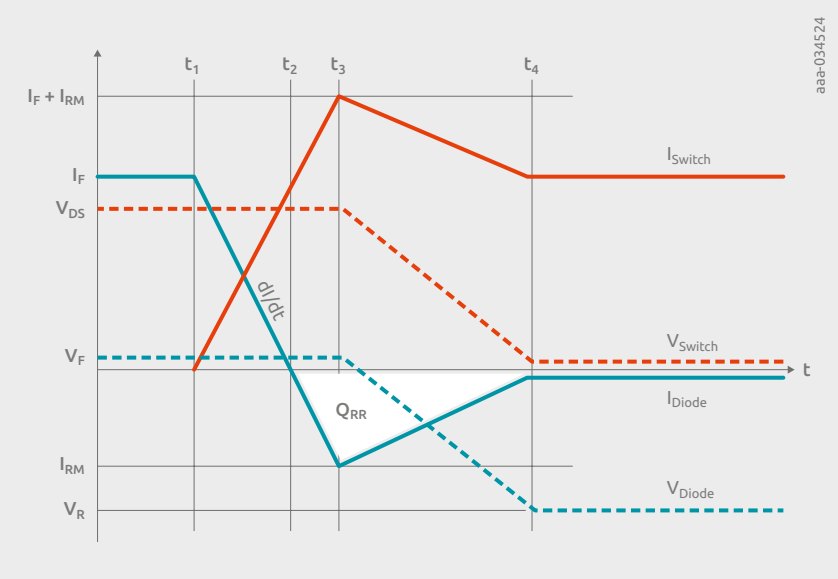


Figure 15 | Graph showing current and voltage waveforms of a diode and the associated switch during the diode turn-off phase.

Figure 14 shows a double pulse testing circuit. Double pulse testing is the standard method for measuring the switching performance of a semiconductor device. It consists basically of a switch which is used to charge the inductance with magnetic energy. By adjusting the width of the first pulse, the required current through the inductance is set while the diode is biased in reverse direction. Then the switch is turned off and the second pulse turns on the device under test (DUT). At this point, the turn-on behavior of the diode can be investigated (forward recovery). Now the current is flowing through the diode. At a given point, t_1 as shown in Figure 15, the switch turns on and starts to turn off the current through the diode with the defined di/dt ramp. As discussed, the diode current will even turn negative and intersects the x-axis at t_2. At this point the switch is still carrying the entire input voltage. Only at time t_3 is the maximum reverse current reached and the space-charge region of the diode begins to form. Now the diode starts to take over the voltage. From this point on, power loss needs to be dissipated in the diode, contributing to switching losses of the circuit. As seen at t_3 the switch must not only carry the current I_F, but also the recovery current I_{RM} of the diode, which increases the switching losses in the switch further. At t_4 the space-charge region in the diode is fully built up and the reverse voltage across the diode equalizes to the input voltage.

2.5 Benchmarking of different technologies in terms of switching

In this section the switching behavior of different diode technologies will be presented and discussed. As an informative introduction, the operating points and evaluation parameters as well as their calculation method are first presented.

2.5.1 Evaluation parameters

Unlike the operating parameters which are manually set beforehand, evaluation parameters are extracted and calculated from the measured current trajectory. They directly represent the switching performance.

Figure 16 shows an approximated reverse recovery current trajectory. The corresponding explanation of the numbers provides the definitions of the evaluated parameters which were extracted and used for the evaluation of the diode performances (which are number 1 to 5).

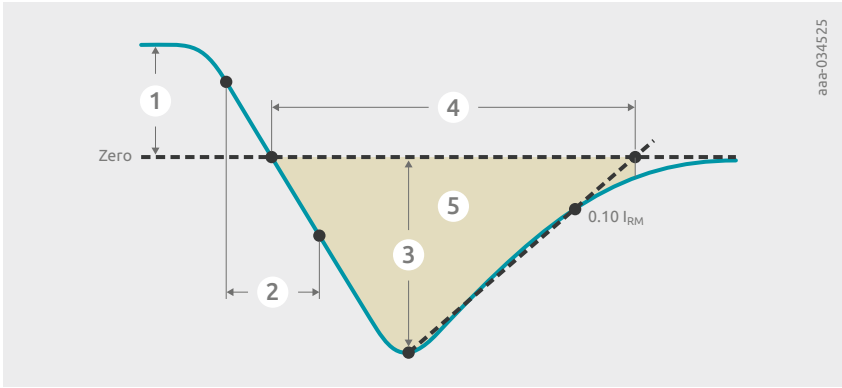


Figure 16 | Schematic of the reverse recovery trajectory with the corresponding parameters.

1. I_F – Forward conduction current
2. di_F/dt – Rate of diode current change through zero crossing
3. I_{RM} – Maximum reverse recovery current
4. t_{rr} – Reverse recovery time, measured from zero crossing where the diode current changes from positive to negative, to the point at which the straight line through I_{RM} and 10% of I_{RM} passes through zero (10% level used for following measurements).
5. Q_{rr} – Reverse recovery charge: area under the curve defined by I_{RM} and t_{rr}
6. Softness factor SF_{rr} – Quotient of di/dt before I_{RM} occurs divided by di/dt after I_{RM} occurs

Operating points – switching performance

The following list gives an overview of the different parameter variations under which the reverse recovery was measured and compared:

Units for all the following tables of the evaluation parameters:

- Q_{rr} is given in [nC]
- I_{RM} is given in [A]
- t_{rr} is given in [ns]
- SF_{rr} is dimensionless

Different parameter variations				
Current edge steepness (in A/ns)	−0.4 (±20%)	−0.7 (±20%)	−1 (±20%)	
DC link voltage (in V)	24	48	75	90
Turn-off current (in A)	1	3	5	
Case Temperatures (in °C)	−40	25	85	150

Please notice that there is a 'cross-influence' of the listed operating parameters. As an example, the turn-off current proportionally increases the current edge steepness di/dt, without any other changes in the gate circuit. Once the influence of changing the turn-off current or dc-link voltage exceeds a set limit, the gate resistor must be adjusted in order to guarantee as similar slope gradients as possible. Therefore, small variations in the di/dt values can be avoided. For that reason, the edge steepness parameters are given in ranges in which the di/dt values were held for the specific measurements. Nevertheless, comparability in the following measurements is guaranteed within each set of measurements, as the operating conditions were absolute equal and therefore free of di/dt variations or other cross-interferences. Here, a set is defined as the measurement of all diodes at the same operating point.

2.5.2 Sample selection

The different diode technologies investigated in this section are: silicon germanium, Trench Schottky, Planar Schottky and reverse recovery diode. Table 1 summarizes the chosen products.

Naturally, the competing devices for analysis were selected to have as similar operating ranges as possible and the same packaging (SOD128). As no 100V recovery rectifiers were available for the chosen current range, 200V types were used instead.

Table 1: Rated current and voltage of the compared devices.

Product	Technology	Voltage / current Rating	Package
PMEG120G30ELP	Silicon germanium	120V / 3A	SOD128
PNE20030EP	Hyper fast recovery	200V / 3A	SOD128
RB058LAM150TR	Planar Schottky	150V / 3A	SOD128
PMEG100T30ELP	Trench Schottky	100V / 3A	SOD128

2.5.3 Impact of temperature on the switching performance

Figure 17 depicts the forward current I_F during the transition from forward bias into reverse direction for a dc-link voltage of 48V and a turn-off current of 3A, at room temperature and at 150°C case temperature. Only the temperature as an operating parameter was varied as stated below. The key factor in this comparison is the very steep current slope of di/dt = −1A/ns which is very close to the real application and 5 to 10 times higher compared to usual test conditions in datasheets.

Fixed operating parameter:
V_{dc} = 48V
I_F = 3A
di/dt = −1 (±20%)

Varied operating parameter:
Case temperature –
T_c = [−40°C, 25°C, 85°C , 150°C]

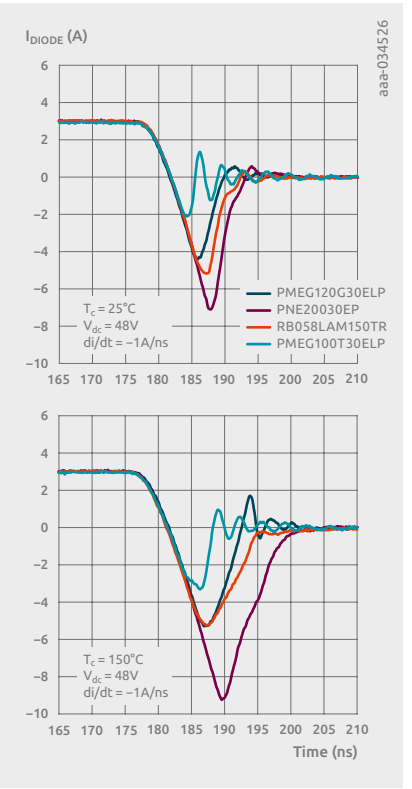


Figure 17 | Reverse recovery current for different technologies at room temperature and at 150°C case temperature.
V_{dc} = 48V, I_F = 3A and di/dt = −1A/ns.

Table 2 lists the corresponding evaluated parameters Q_{rr}, I_{rrm}, t_{rr} and SF_{rr} which were derived from the figures above.

Units for all the following tables of the evaluation parameters:

- Q_{rr} is given in [nC]
- I_{RM} is given in [A]
- t_{rr} is given in [ns]
- SF_{rr} is dimensionless

Table 2: Reverse recovery evaluation parameters for different temperatures. Other operating parameters kept constant at V_{dc} = 48V, I_F = 3A and di/dt = –1A/ns.

Product	Q_{rr} @ T =				I_{RM} @ T =			
	–40°C	25°C	85°C	150°C	–40°C	25°C	85°C	150°C
PMEG120G30ELP	13.6	19.1	25.5	33.1	4.02	4.42	4.87	5.3
PNE20030EP	25.8	37.3	52.1	80.5	6.28	7.11	8.12	9.24
RB058LAM150TR	11.9	26.3	33.5	41.6	5.18	5.18	5.2	5.25
PMEG100T30ELP	4.8	4.7	6.8	14	2.3	2.1	2.3	3.32

Product	t_{rr} @ T =				SF_{rr} @ T =			
	–40°C	25°C	85°C	150°C	–40°C	25°C	85°C	150°C
PMEG120G30ELP	6.4	8.24	9.7	11.2	0.66	0.87	0.94	0.96
PNE20030EP	8.2	11.1	13.6	18	0.59	0.82	0.94	1.17
RB058LAM150TR	5.3	10.6	12	14.2	0.36	1	1.19	1.37
PMEG100T30ELP	3.6	3.8	4.9	6.9	0.36	0.42	0.44	0.34

Key observations

For nearly all operating points, the Trench Schottky diode outperforms all other competing diodes. This holds for Q_{rr}, I_{RM} and t_{rr} values. As a trade-off compared to the other technologies, the Trench Schottky diode shows a higher snappiness and subsequent oscillation. It is also remarkable that the 120V SiGe diode has less stored charge than the 150V planar Schottky diode, in spite of the very low leakage current that this product has. As expected, the hyper fast recovery rectifier switches the slowest and has the highest amount of stored charge. Here the bipolar nature of the hyper fast diode becomes noticeable despite the life-time killing material in the epitaxial layers. However, one should also note the smooth switching of this hyper fast diode.

2.5.4 Why is the Trench Schottky diode superior in terms of switching

The measurements in Figure 17 illustrate the superior performance of Trench Schottky diodes in terms of switching when compared to all other technologies. A look at the data sheets shows that the Trench Schottky diode even shows the highest parasitic capacitance compared to all the other products. In this respect the question arises how this happens. The answer can be found in Figure 8. As shown in the cross section, there is no guard ring in the termination design for the 100V Trench Schottky diodes. The impact can be best be investigated by using physical device simulations. For this reason, the switching behavior of the planar Schottky diode PMEG10030ELP and of the Trench Schottky diode PMEG100T030ELP was simulated. The simulated switching performance is illustrated in Figure 18. Device simulations confirm the measured superior switching performance of the Trench Schottky diode PMEG100T030ELP compared to its planar counterpart PMEG10030ELP. In the device simulation it is easy to omit the guard ring of the planar Schottky diode and to investigate the impact of the guard ring on the switching performance. The blue curve in Figure 18 shows the planar diode without the guard ring. In fact, the planar Schottky diode without guard ring is now approaching the Trench Schottky diode. However there is still a gap between the planar Schottky diode without guard ring and the Trench Schottky diode in terms of Q_{rr} and t_{rr}. Obviously, the missing guard ring in the Trench Schottky device can explain a large part of the difference, but not all. The second factor why the Trench-Schottky diode switches much faster and with less stored charge is the significant size difference of the active areas. For a fair comparison of the die sizes, it is necessary to subtract the dead area caused by the trenches from the active area of the Trench Schottky diode, comparing only the effective active area that really contributes to the forward current to that of its planar counterpart. This is shown in Figure 19. This way to compare the active areas reveals that the Trench Schottky PMEG100T030ELP occupies only 44% of the active area of its planar counterpart PMEG10030ELP. In summary, the superior switching behavior of the Trench Schottky diode can be explained by the lack of a guard ring with a parasitic pn junction and by its much smaller active area compared to other devices. Please notice that the impact of the guard ring on the switching behavior is very much die size dependent, as the area of the guard ring with a fixed width increases linearly, while the active area itself increases exponentially with increasing die pitch. So the bigger the die size the less pronounced is the impact of the guard ring on the switching performance. The influence of the guard is also dependent on how far the diode is biased in the forward direction, and thus how much the guard ring is triggered to conduct current. We will see in 2.5.6 that this has a huge impact on the switching performance.

The reason for the switching behavior is now clarified. But the question still remains: why is the parasitic capacitance of Trench Schottky diode so large and why it is not affecting the switching performance? This can again be answered with a look at the cross section of the device. The cross section of a Trench unit cell is shown in Figure 20, together with the resulting equivalent circuit diagram of the cell. In this Figure one can see the parasitic capacitance C_{diode} that exists in each Schottky diode due to the metal-semiconductor junction in the device. However, with Trench Schottky diodes there is a second parasitic capacitance in the device structure. Called C_{Trench}, this capacitance is caused by the thin dielectric in the trenches which are filled with poly silicon. This high parasitic capacitance contributes to the overall parasitic capacitance of the Trench Schottky diode, resulting in a high specified parasitic capacitance in the data sheet. However the parasitic capacitance C_{Trench} can be quickly charged and discharged through the highly doped poly silicon layer in the trenches. It is not affected by the dynamics of charge carriers in the drift region, which is the case for the capacitance C_{diode}.

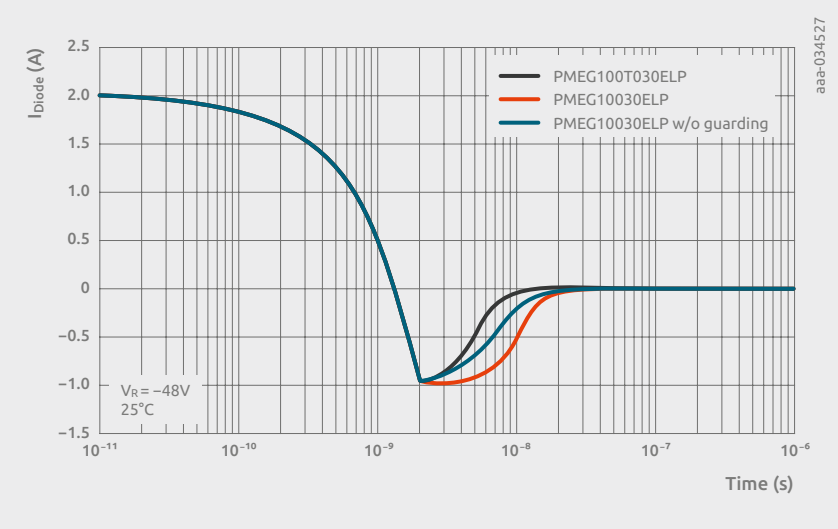


Figure 18 | Simulated ramp reverse recovery of three different diodes. PMEG100T030ELP (Trench Schottky), PMEG10030ELP (planar Schottky) and PMEG10030ELP without guard ring.

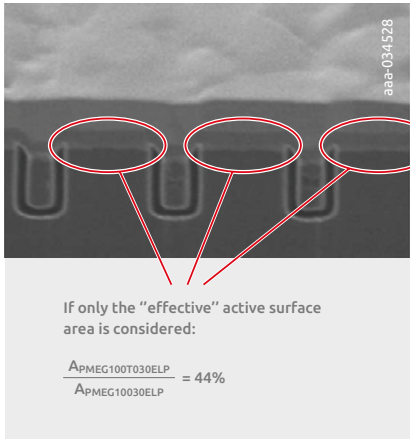


Figure 19 | For a fair comparison of the die sizes, only the effective active areas should be compared. Using this method to compare active areas reveals that the Trench Schottky PMEG100T030ELP occupies only 44% of the active area of its planar counterpart PMEG10030ELP.

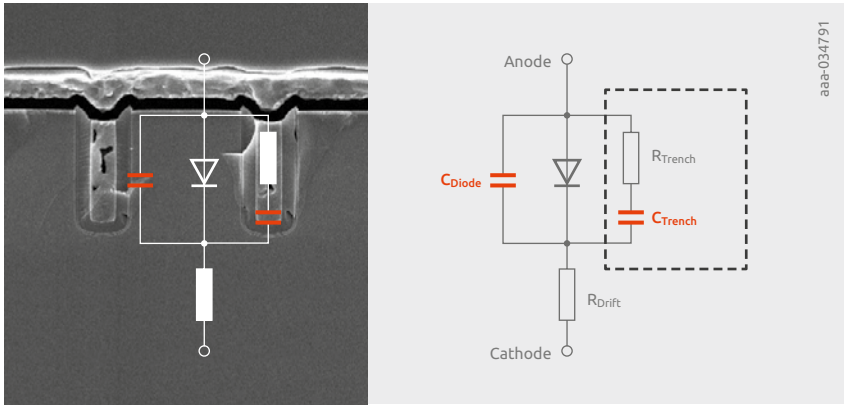


Figure 20 | Cross section of a unit cell in a Trench Schottky diode and the resulting equivalent circuit diagram of the Trench Schottky diode. The thin dielectric in the Trenches contributes to a high overall parasitic capacitance of the Trench Schottky diode.

2.5.5 Impact of the slope gradient on switching performance

In this section the reverse recovery process is evaluated for different values of the slope steepness di/dt. Figure 21 shows the decrease to di/dt = –0.4A/ns as a reference. The quantified parameter including the ones for di/dt = –0.7A/ns are listed in Table 3.

Fixed operating parameter:
V_{dc} = 48V
I_F = 3A
T_c = 25°C

Varied operating parameter:
Slope steepness:
di/dt = –0.4A/ns
di/dt = –0.7A/ns

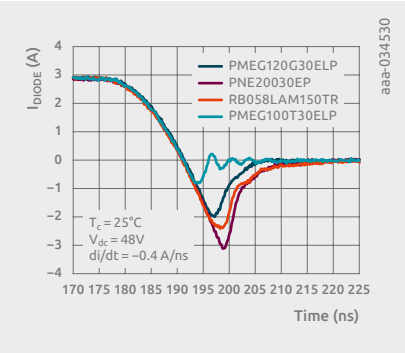


Figure 21 | Reverse recovery current for lower current slope steepness of –0.4A/ns. Other operating parameters kept constant at V_{dc} = 48V, I_F = 3A and T_c = 25°C.

Table 3: Reverse recovery evaluation parameters for slope steepness.

Other operating parameters kept constant at V_{dc} = 48V, i_F = 3A and T_c = 25°C.								
Product	Q_{rr} @		I_{RM} @		t_{rr} @		SF_{rr} @	
A/ns	–0.4	–0.7	–0.4	–0.7	–0.4	–0.7	–0.4	–0.7
PMEG120G30ELP	12.6	15.4	2	2.8	13.4	11.4	1.5	1.3
PNE20030EP	22.7	28.3	3.1	4.4	16.8	14.6	1.2	1.1
RB058LAM150TR	20	22.7	2.4	3.3	18.7	14.6	1.7	1.4
PMEG100T30ELP	2.5	3.3	0.8	1.3	5	4.4	0.78	0.5

Key observations

The Trench Schottky diode also remains superior to all competing technologies at lower switching speeds. Nothing else changes in the order in terms of switching speed and amount of stored charge, with SiGe in second place and planar Schottky and hyperfast diode in third and fourth place.

2.5.6 Impact of the turn-off current on switching performance

The diodes were also tested for different turn-off currents. The turn-off current has a significant influence on the di/dt and therefore on the reverse recovery process. Figure 22 illustrates the reduced turn-off current of 1A. The evaluated parameter for a higher turn-off current of 5A where no ranking changes occur, is listed in Table 15.

Fixed operating parameter:
V_{dc} = 48V
T_c = 25°C
di/dt = –1 (±20%)

Varied operating parameter:
Turn-off current:
I_F = [1A ; 5A]

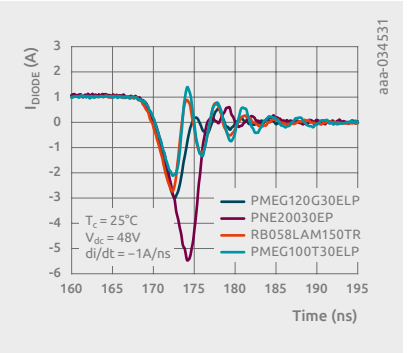


Figure 22 | Reverse recovery current for 1A turn-off current. Other operating parameters kept constant at V_{dc} = 48V, T_c = 25°C and di/dt = –1A/ns.

Table 4: Reverse recovery evaluation parameters for different turn-off current.

Other operating parameters kept constant at V_{dc} = 48V, T_c = 25°C and di/dt = - 1A/ns.								
Product	Q_{rr} @		I_{RM} @		t_{rr} @		SF_{rr} @	
i_F =	1A	5A	1A	5A	1A	5A	1A	5A
PMEG120G30ELP	7.5	31	3	6.1	4.7	9.4	0.73	0.74
PNE20030EP	17.6	50.6	5.5	8.6	6.4	12	0.5	0.77
RB058LAM150TR	5.5	49	2.7	7.4	3.8	12.3	0.4	0.88
PMEG100T30ELP	4.3	6	2.1	2.6	3.4	4	0.36	0.4

Key observations

The investigated products have a nominal current rating of 3A. The higher turn-off current results in a higher forward voltage drop, triggering the parasitic pn junction in the termination area even more. Therefore, as shown in Table 4 there is a significant increase at 5A turn-off current for all diode technologies that use the guard-ring as termination concept in terms of Q_{rr}, I_{rrm} and t_{rr} values. The impact on Trench Schottky diodes is much less pronounced due to the lack of pn junction in the device structure. At the same time, it is also very important to note that at

lower turn-off current of 1A (well below the current rating of the products) the advantage of the Trench-Schottky diode diminishes, as the parasitic pn diode loses importance in the structure of the other diodes. As shown in Table 4 for 1A turn-off current, the planar Schottky product is almost on par with the Trench Schottky in terms of Q_{rr}, I_{rrm} and t_{rr}. This is consistent with the simulation results discussed in 2.5.4. Consequently, depending on the current level and the current density of the device, in addition to the switching frequency, duty cycle and temperature, the optimal diode technology for each application may be a different one.

In summary, next to ambient temperature, the turn-off current has the greatest influence on switching behavior of the diodes and should be taken into account during circuit design.

2.5.7 Impact of the reverse voltage on switching performance

In this section, the variation of the dc-link voltage is investigated and presented. The reverse voltage during the switching process is depicted on the right side in Figure 23 next to the corresponding current trajectory. Quantified results are presented in Table 5.

Fixed operating parameter:
$I_F = 3A$
$T_c = 25°C$
$di/dt = -1A/ns$ (±20%)

Varied operating parameter:
dc link voltage:
$V_{dc} = [48V ; 90V]$

Table 5: Reverse recovery evaluation parameters for different dc-link voltages V_{dc}

Diode		Q_{rr} @		I_{RM} @		t_{rr} @		SF_{rr} @	
	V_{dc}=	75V	90V	75V	90V	75V	90V	75V	90V
PMEG120G30ELP		19.3	19.3	4.1	4.1	8.6	8.9	0.93	0.74
PNE20030EP		38.1	37.9	6.8	6.6	12	12.3	0.93	0.96
RB058LAM150TR		27.3	27.4	5	4.8	11.1	11.3	1.1	1.1
PMEG100T30ELP		4.5	4.5	2	1.9	3.8	3.8	0.42	0.45

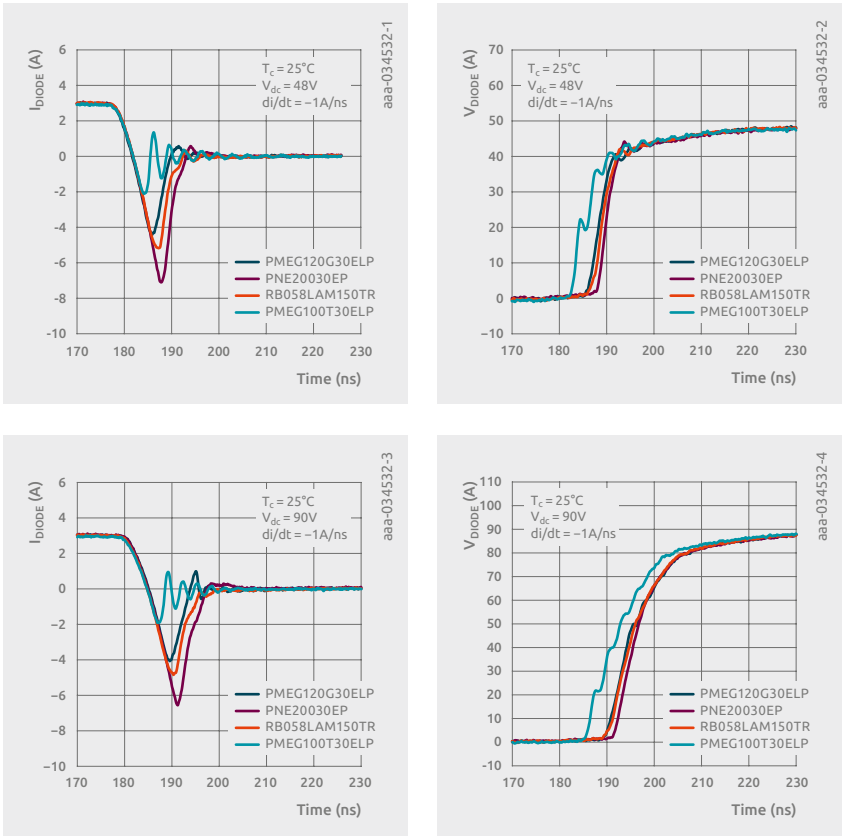


Figure 23 | Reverse recovery and reverse voltage for different dc-link voltages.
Fixed operating parameters $I_F = 3A$, $T_c = 25°C$, $di/dt = -1A/ns$

Key observations

The trajectories of the voltages are consistent with the corresponding current curves, both in terms of oscillation and slope steepness. The performance ranking among the diodes remains unchanged from the first observations with the Trench Schottky diodes being dominant in terms of Q_{rr}, I_{rrm} and t_{rr}. The 120V SiGe product takes second place and remains ahead of the Planar Schottky and the hyper fast recovery diodes.

2.6 SiC rectifier

2.6.1 Introduction

Silicon carbide, often simply abbreviated as SiC, is a compound semiconductor that consists of both silicon and carbon atoms. Unlike other materials, silicon carbide exists in many crystal structures. This phenomenon is called polymorphism. For SiC, more than 250 different polytypes are known. Each polytype has its own unique properties. For commercial power electronic power devices, the polytype 4H-SiC is predominantly used. The arrangement of a 4H-SiC crystal is depicted in Figure 24.

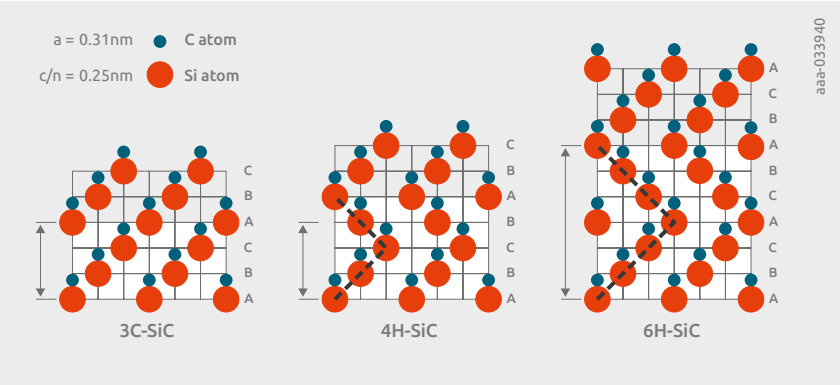


Figure 24 | SiC polytypes

4H-SiC crystal structure, later simply called SiC, has several material benefits over silicon. These are leveraged in modern high voltage diodes to specifically create high performance diode solutions for switched-mode power conversion applications. Significant application examples include:

- Switched-mode Power Supplies (SMPS)
- On-Board Chargers (OBC)
- Inverters (Traction & Photovoltaic)
- Charging Stations
- Electric Aircraft Propulsion
- Uninterruptible Power Supplies (UPS)

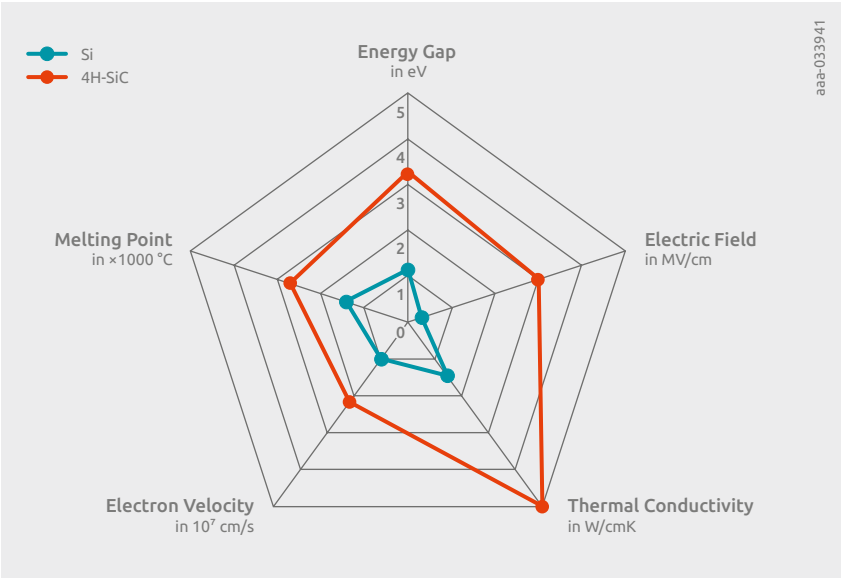


Figure 25 | Comparison of Si and SiC material properties.

2.6.2 Material properties of 4H-SiC

Compared to Si and as depicted in Figure 25, SiC has an energy gap around three times higher, and a ten times higher dielectric breakdown field strength. The electron velocity is also more than twice as high as it is for silicon. Besides these electrical benefits, the thermal performance of SiC is also advantageous. Both the thermal conductivity (SiC 4.9W/cmK vs Si 1.5W/cmK) and also the melting point (SiC 2700°C vs Si 1400 °C) are much higher.

These superior material properties are utilized to manufacture power semiconductors which exceed the performance of their Si-based counterparts and permit operation even under harsh environmental conditions.

As far as power diodes are concerned, the combination of the ten times higher dielectric breakdown field strength and the nearly three times higher energy gap are utilized for a new sort of power diode which is perfectly-made for switch-mode applications. A detailed description on how SiC's material advantages positively affect power diodes' performance will follow in the next section.

2.6.3 SiC enabling superior power diodes and changing the high voltage diode landscape

As a consequence of SiC's ten times higher dielectric breakdown field strength, a much thinner drift layer is sufficient to achieve the same blocking voltage, as compared to silicon-based devices. A simplified explanation is shown in Figure 26, assuming a Schottky-metal contact for both silicon and silicon carbide materials. Another aspect refers to the possible higher doping concentration which lowers the resistance of the already thinner drift layer even more. In theory, SiC can reduce the resistance per unit area of the drift layer to 1/300 of that of Si for the same breakdown voltage. Therefore, at a given current rating, SiC diodes can be manufactured with a lower voltage drop and smaller die size. This results in better conduction, and also, due to the smaller die size and lower switching charge, faster switching time and lower switching losses. These SiC benefits become technically and commercially relevant at blocking voltages of 600V and above.

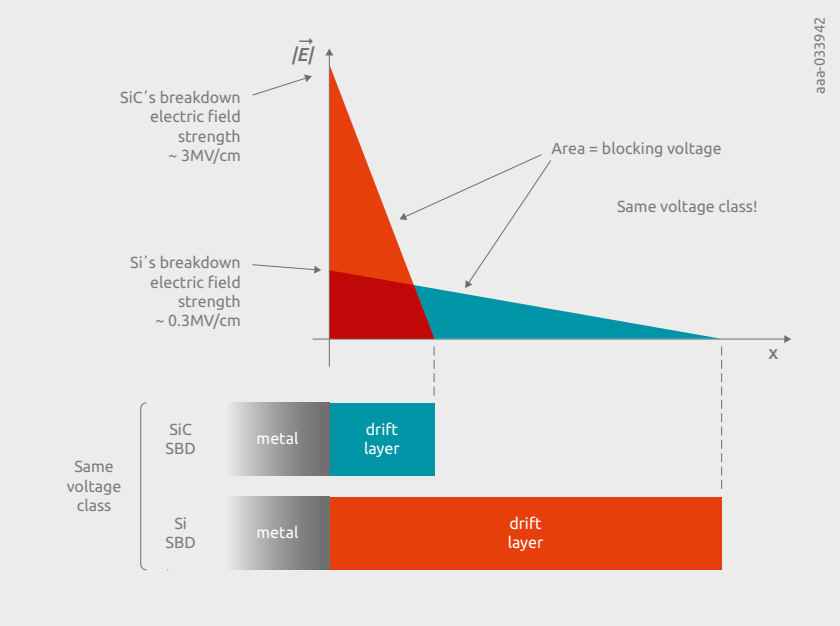


Figure 26 | SiC dielectric field strength and energy gap advantage.

Figure 27 shows the split between Si and SiC diode technologies against blocking voltage. On the left, conventional Si-based technologies are depicted. In the Si-domain and below 100V diodes utilizing the advantageous properties of Schottky-metal contacts are usually the dominant solution. They offer a very low cut-in voltage and, due to the majority carrier based conduction mechanism, an almost purely capacitive – and therefore very fast – switching behavior. Between 100V and 200V the leakage currents and thus the thermal stability of Si Schottky diodes becomes more and more challenging to control. Additionally, the influence of the drift layer resistance rises significantly so that at a blocking voltage range of around 100V to 200V, the transition from Schottky-based diodes towards PN-based diodes takes place. Due to the bipolar nature of PN diodes, the thermal stability is higher compared to unipolar devices. However, due to the presence of minority carriers, stored charges lead to reverse recovery effects, higher switching times and thus higher losses in switched-mode operation. Therefore, in silicon and at blocking voltages of 600V and above, only PN-based rectifiers are available. Switched-mode applications in this voltage range must, therefore, deal with the mentioned disadvantages of the silicon PN diodes. As a consequence, the efficiency of certain power applications cannot be further improved because Si-based PN diode solutions have reached their physical limitations.

On the other hand, with SiC and its higher energy gap, Schottky power diodes can still be manufactured with low leakage current and high thermal stability at blocking voltage levels of 600V and above. As a consequence, SiC allows the exploitation of the advantages of unipolar Schottky-contact based power diodes in voltage ranges where Silicon-based power diode counterparts are already bipolar devices. This means that at blocking voltage levels between 600V and 1700V, SiC can make use of its two major advantages compared to Silicon, the lower voltage drop and the better switching performance. Firstly, this is originated by the thinner drift layer and smaller die sizes at a given current as already shown in Figure 26. The drawback of the higher energy gap and the resulting high cut-in voltage is compensated with the much smaller required drift layer and the utilization of the Schottky-diodes' semiconductor-metal junction.

Secondly, consider the ability to continue to make use of Schottky diode structures at blocking voltage levels where silicon-based diodes are bipolar PN diodes. This minimizes switching losses due to the absence of the comparably higher reverse recovery charge compared to the lower capacitive charge of Schottky diodes. Consequently, SiC Schottky diodes offer faster switching times than Si-based competing diodes without compromising the conduction performance and the stability.

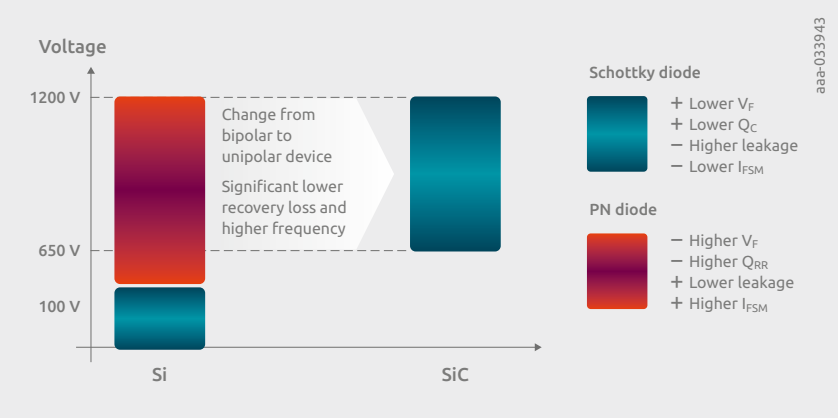


Figure 27 | Comparison of Si and SiC power diodes vs blocking voltage.

Although pure SiC-based Schottky devices have a comparably low forward voltage drop V_F and fast switching times, the imperfections at the metal-semiconductor interface lead to leakage currents higher than theoretically expected. Additionally, the unipolar nature makes these devices susceptible to surge current situations such as load dumps or line drop outs. As a consequence, a pure SiC Schottky diode concept doesn't allow the exploitation of SiC's full potential.

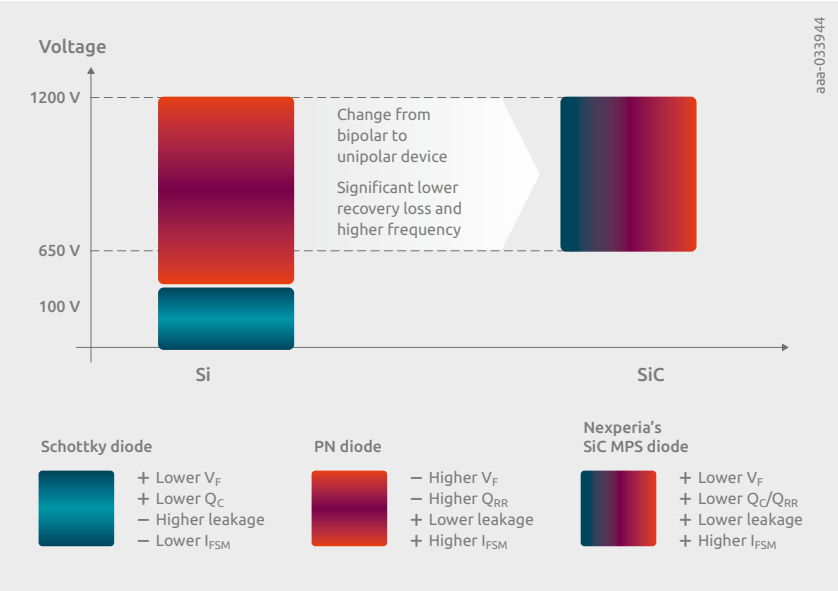


Figure 28 | SiC MPS diode.

In order to overcome the drawbacks of pure SiC Schottky diodes, Nexperia has designed a hybrid SiC diode concept which combines the best of both worlds, see Figure 28. The result is a product with the superior conduction and switching performance of Schottky diodes and the higher thermal stability and surge current robustness of bipolar diodes. This hybrid diode is called 'Merged PIN Schottky' or MPS. A detailed explanation of the functionality of MPS diodes is given in the next section.

Merged PIN Schottky (MPS): A closer look into high-end silicon carbide power diodes

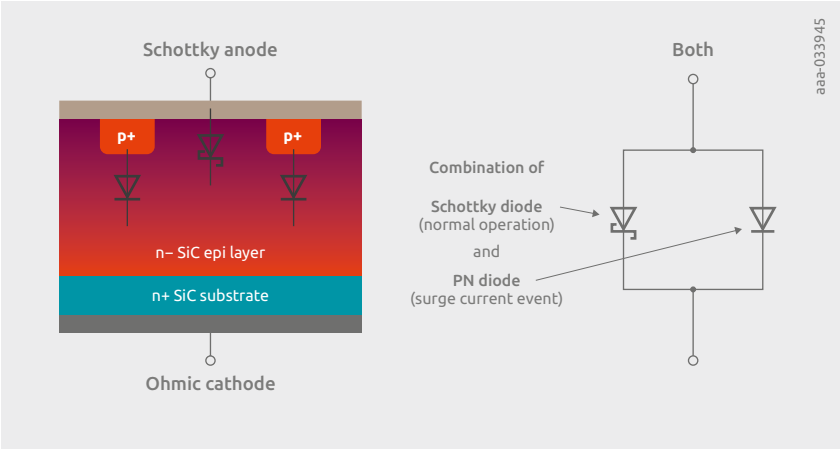


Figure 29 | Simplified "Merged PIN Schottky" diode cross section and equivalen circuit.

A simplified cross section of an MPS diode is shown in Figure 29. Unlike pure Schottky devices, MPS diodes do not only possess a metal-semiconductor interface. P-doped areas are also embedded within the drift zone which form a p-ohmic contact with the metal at the Schottky anode and a PN junction with the lightly n-doped SiC drift or epi layer. As depicted in the equivalent circuit in Figure 29, an MPS diode monolithically possesses both a Schottky diode and a PN diode portion. Both diodes contribute to the overall current depending on the mode of operation. This will be described in detail later.

MPS in blocking operation

Another aspect of the MPS diode contributes to the blocking behavior. As shown in Figure 30, the p-areas (also often called p-pillars or p-wells) stabilize such diodes and reduce the leakage currents under reverse bias.

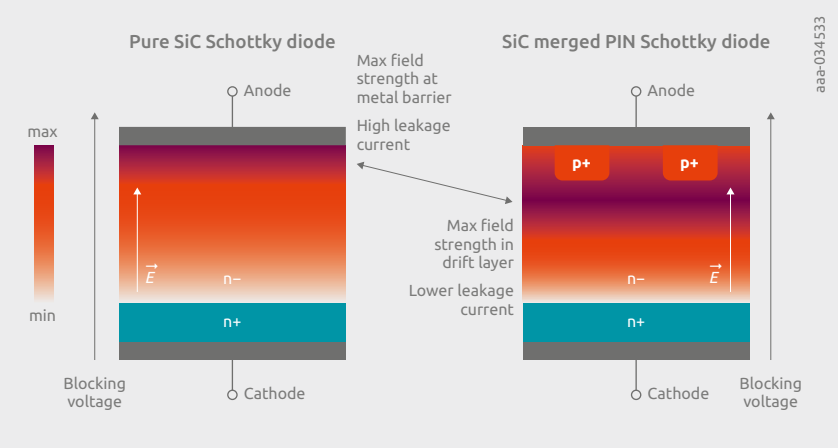


Figure 30 | Comparison of e-field distribution of pure Schottky diodes & MPS at reverse bias.

The electric field strength distribution during reverse bias situations is depicted in Figure 30 on the left-hand side, for a pure Schottky configuration. From the cathode side, the electric field strength gradually extends across the drift layer and reaches its peak at the metal-semiconductor interface at the anode side. Consequently, the maximum electric field strength occurs at a location where a comparably high density of defects and imperfections are present. As a consequence, these pure Schottky devices possess a relatively high leakage current which can only be countered with a thicker drift layer than should theoretically be needed. However, this is disadvantageous for lowest drift-resistance and hence for diodes for power electronic applications.

The inserted p-areas in the MPS structure dramatically change the electric field strength distribution compared to a pure Schottky structure. This is shown in the right-hand cross section of Figure 30. The depletion regions of the adjacent PN junctions caused by the inserted p-areas deflect the maximum field strength, which is shifted away from the metal interface into the drift layer region. The almost defect-free area of this layer and the significantly reduced electric field strength stress at the metal interface at the anode side significantly reduce the leakage current compared to a pure Schottky counterpart of the same geometry and same applied reverse voltage. The effectiveness of this pinch-off is determined by the relative area and geometrical layout of the p-area implant, its doping

concentration, the spacing between adjacent p areas as well as the encompassed Schottky area, and its metal-SiC barrier height. These are fundamental design parameters that affect the device characteristics. A large p+ implanted area is expected to result in a higher on-state voltage due to a smaller Schottky conducting area, but may offer lower leakage due to a more effective pinch-off of the Schottky portion. Alternatively, by keeping the leakage current and the geometry of both – the pure Schottky diode and the Merged PIN Schottky diode – the MPS diode can operate at higher breakdown voltages without expanding the drift layer and the associated drift resistance, which is electrically beneficial for power applications in particular.

MPS in nominal forward operation and overcurrent events

As previously mentioned, the inserted p-areas not only relieve the electric field strength stress at the metal-semiconductor interface under reverse bias situations to lower the leakage current. The associated pn junctions of the p-areas are also designed such that they can also carry significant current in forward bias situations. This feature is used to overcome the limitations of unipolar devices with their comparably higher differential resistances compared to bipolar counterparts at a given crystal size. In Figure 31, the MPS cross section, the equivalent circuit and the I-V-curves of a pure Schottky, a pure PN and a MPS diode is shown as examples. As shown in Figure 29 and Figure 31, an MPS diode possesses two monolithically integrated diodes, the Schottky and the PN diode.

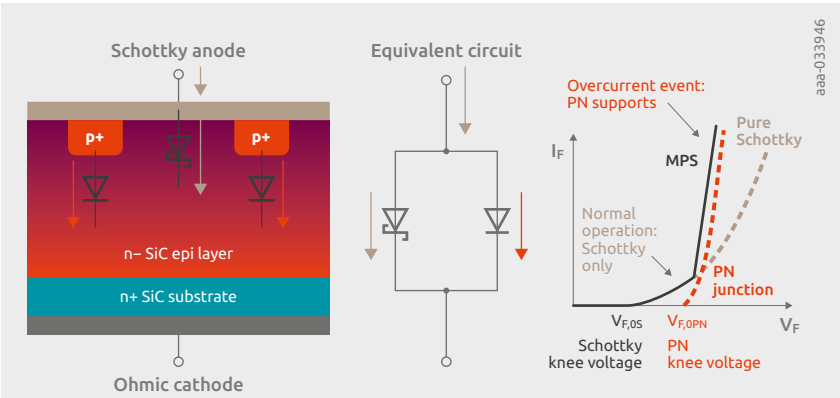


Figure 31 | Merged PIN Schottky diodes under nominal and overcurrent situation.

Under nominal current conditions, the voltage drop of the MPS is so low that only the Schottky area actively contributes to the overall current, and the integrated PN diode remains inactive. This is indicated as the green current in the equivalent circuit in Figure 31, where the forward current is only conducted through the Schottky area of the MPS diode under a certain threshold. This is called 'unipolar mode' and the device acts in pure Schottky mode with a low cut-in voltage and purely capacitive switching performance. The corresponding low cut-in voltage of the Schottky area and the PN junctions of the MPS area are indicated in the I-V-curve in Figure 31.

Typical I-V-curves of a SiC MPS under nominal current conditions at different junction temperatures are depicted in Figure 32. Nominal current conditions can be assumed for the majority of switched-mode applications of such devices. The SiC diodes possess three different areas in the I-V-curve with different temperature dependencies with NTC, ZTC and PTC behavior.

In the lower current range, the SiC diodes' cut-in voltage decreases with increasing junction temperature, resulting in an NTC behavior. With increasing current, the drift resistance becomes more relevant. As a result, there is an I-V-point which has no temperature dependency. All I-V-curves at different junction temperatures intersect at this point. This point possesses a zero temperature coefficient (ZTC) and indicates the transition from NTC to PTC diode behavior. As illustrated in Figure 32, the steepness of the I-V-curves decline with increasing junction temperature. At currents above the ZTC point, the device shows a clear PTC behavior enabling parallelization of SiC diodes for applications with higher current demand.

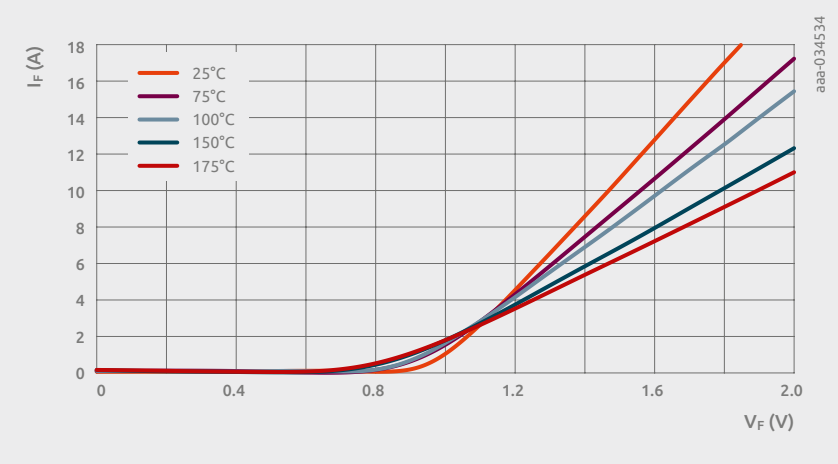


Figure 32 | Temperature dependency onto the static I-V-curve of a SiC MPS under nominal current conditions.

However, if we extrapolate the I-V-curve of a pure Schottky device, the comparably high differential resistance of unipolar devices is disadvantageous. Particularly in the presence of high current exceeding the nominal current range, the comparably high differential results in high on-state losses and poor over-current capability. To overcome this drawback at transient high-current situations such as surge currents, pure Schottky devices need to be paralleled to handle these currents. In real-world applications the diode selection often must be over-dimensioned purely for this transient situation. This is often disadvantageous from a commercial and also a performance perspective. The MPS design overcomes the drawback of devices with pure forward Schottky behavior.

The PN diode of the MPS structure behaves exactly diametrically to the Schottky diode. The initial cut-in voltage of the monolithically-integrated PN diode is so high so that under nominal application conditions, this part of the MPS will not contribute to the overall current. Here, the MPS acts as a pure Schottky diode. However, at high forward current situations and due to the comparably high differential resistance of the Schottky area MPS, the voltage drop becomes so high that the integrated PN junction is triggered and holes are injected. According to the equivalent circuit in Figure 31, both diodes carry the current. The formerly pure unipolar device becomes a bipolar device. The injected holes significantly increase the conductivity of the diode resulting in a much steeper I-V-curve and a much higher current-handling capability, and thus higher I_{FSM}. This mode of operation is called bipolar mode.

The static I-V forward performance of an MPS diode including the bipolar mode at over-current events is illustrated in Figure 33. The corresponding dynamic performance when the same diode is stressed with a 10ms sinusoidal current is shown in Figure 34. It can be clearly seen that a superior transient behavior of the MPS diode can significantly relief the thermal stress of the power diode during surge current situations. Not only can this action prevent thermal runaway and destruction of the device, the reduced impact on the junction temperature is also beneficial for the device's lifetime and reliability, and should be taken into consideration during an engineer's parts selection, especially for heavy duty, long-lifetime or safety-relevant applications.

The reason for this beneficial performance can best be described by thoroughly looking at the static I-V-curve at higher currents. Consider the static measurements in Figure 33. The different temperature behavior of both integrated diodes within the MPS structure behave differently. With rising junction temperature, the differential resistance of the Schottky part increases resulting in flatter I-V-curves with increasing temperature. On the other hand, the threshold where the PN diode of the MPS kicks in decreases. From an application perspective this is extremely beneficial since the protective nature of this bipolar mode is even more important at

higher junction temperatures. SiC diodes without the MPS concept, with the same nominal current rating as SiC MPS, show an inferior over-current capability and may not withstand the same over-current as the more robust MPS designs. For specific applications such as power factor correction or power supplies where transient over-currents can occur due to load dumps or line drop outs, hardware designers must factor this into their design considerations. As a consequence, designers have to add a more complex protective circuit to prevent over-currents and/or over-specify when SiC diodes without MPS concept are to be used. Both will negatively affect the cost structure. Nexperia's robust SiC MPS diode solves this issue, reducing system complexity without the need of expensive over-dimensioning.

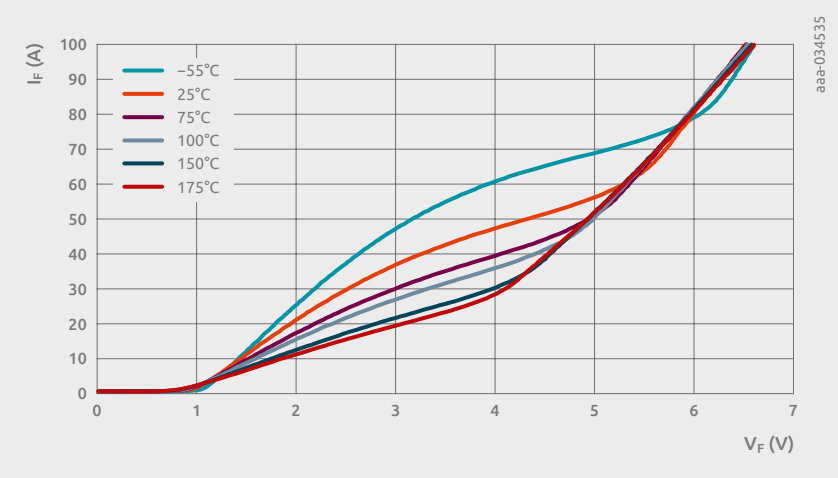


Figure 33 | Static I-V-behavior of SiC MPS diodes including overcurrent.

As individual and application-specific as it is for hardware designer to select the most suitable SiC diode for their power design, so it is for the semiconductor design process of MPS diodes.

The ratio between Schottky area and PN area within an MPS diode correlates with the normal forward conduct capability and the surge current handling. The higher the PN portion of a SiC MPS at a given die size, the higher the over-current capability of the device will be. However, this will adversely affect the low voltage drop under nominal current conditions. Thus, a trade-off must be found between lowest achievable voltage-drop under nominal current conditions and highest possible over-current robustness. The optimum is always application-specific. Nexperia has chosen a trade-off ratio between PN and Schottky width within the SiC MPS diodes which will be most suitable for wide range of hard- and soft-switching applications.

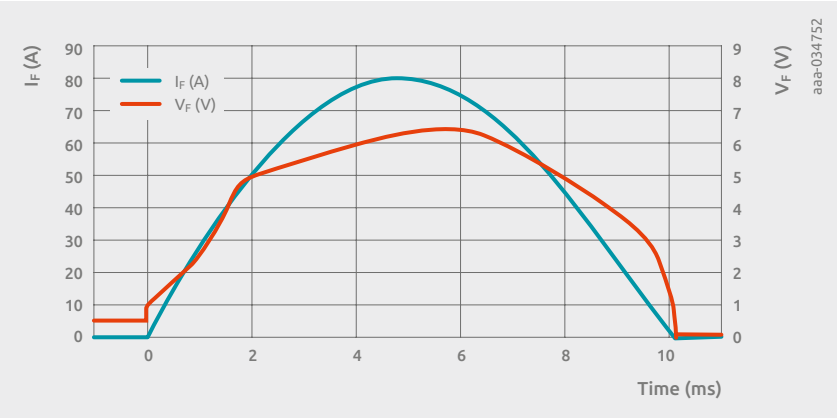


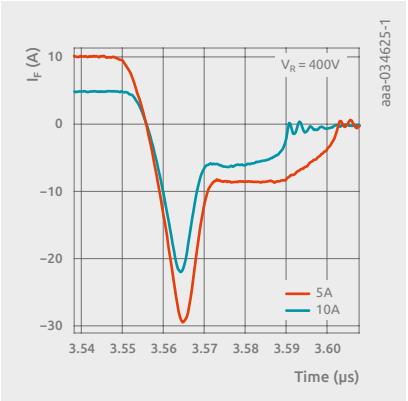
Figure 34 | Dynamic overcurrent behavior during 10ms sinusoidal current stress.

SiC MPS diode's reverse recovery advantage

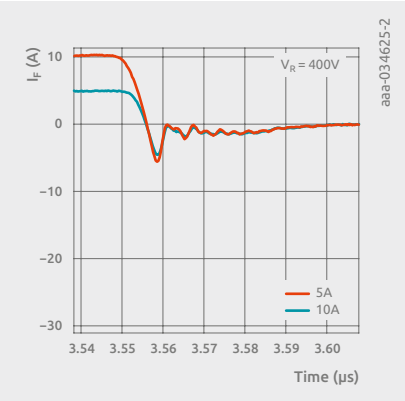
Besides the static advantages, SiC MPS diodes offer advantages during dynamic operation in switching mode. One major advantage over silicon-based PN diodes relates to the reverse recovery behavior. As already described, under nominal conditions SiC MPS diodes behave like Schottky-diodes. Unlike conventional Si fast recovery diodes, only majority carriers contribute to the overall current for SiC diodes. As a result, SiC diodes show a purely capacitive switching behavior, resulting in a lower reverse recovery charge than a Si fast recovery diode with the same electrical rating. The important reverse recovery charge is one of the main loss contributors and thus adversely affects converter efficiency. SiC's reverse recovery charge is not only lower than silicon-based counterparts. In Figure 35 the effects of parameters relevant to converter performance – such as different diode turn-off currents and junction temperatures – are depicted. Obviously, SiC shows an almost constant behavior in the presence of such variations. SiC does not exhibit most of the non-linear behavior of Si fast recovery diodes. Hence, its behavior is easier to predict for power designers because they don't have to take various ambient temperatures and load conditions into consideration. Both diode technologies share the fact that the blocking voltage will affect the capacitive portion of the overall recovery charge. For Si-based PN diodes this portion is comparatively small because the recovery charge is dominated by the stored minority carriers during turn-off of the diode. Hence, the voltage dependence of the capacitive charge is often negligible.

Due to the absence of minority carriers in a SiC diode, the capacitive charge is the only contributor to the reverse recovery charge, and thus causes losses during switching. In Figure 36 the dependency of the applied blocking voltage on the

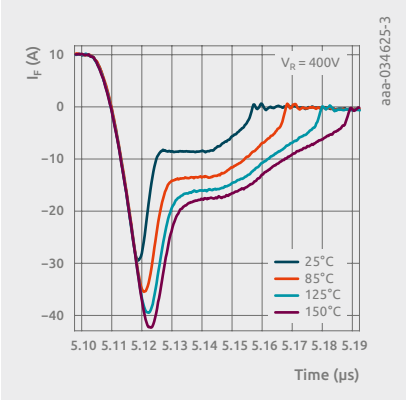
capacitive charges is illustrated. The effective capacitive charge can be extracted from the diode capacitance behavior vs the applied voltage by calculating the area below the capacitance voltage function. As depicted in Figure 36, higher voltages result in higher charge and thus higher stored energy. This capacitive charge of the diode induces losses in the transistor in the switching cell in typical power electronic topologies, and must therefore be taken into consideration during the selection phase of the diode-transistor pair selection. As illustrated in Figure 36, this stored energy is comparably low compared to the reverse recovery charge of Si counterparts. But although this energy is low, it can be become relevant especially in high-frequency converters.



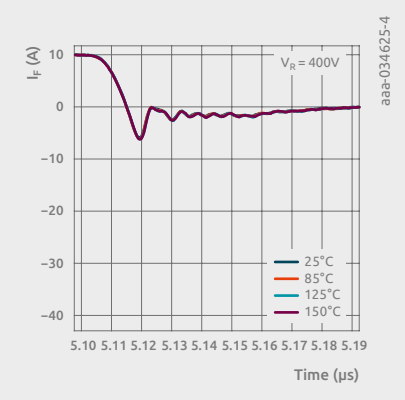
Si diode



SiC diode (PSC1065K)



Si diode



SiC diode (PSC1065K)

Figure 35 | Comparison of reserve recovery behavior of SiC vs. Si diodes.

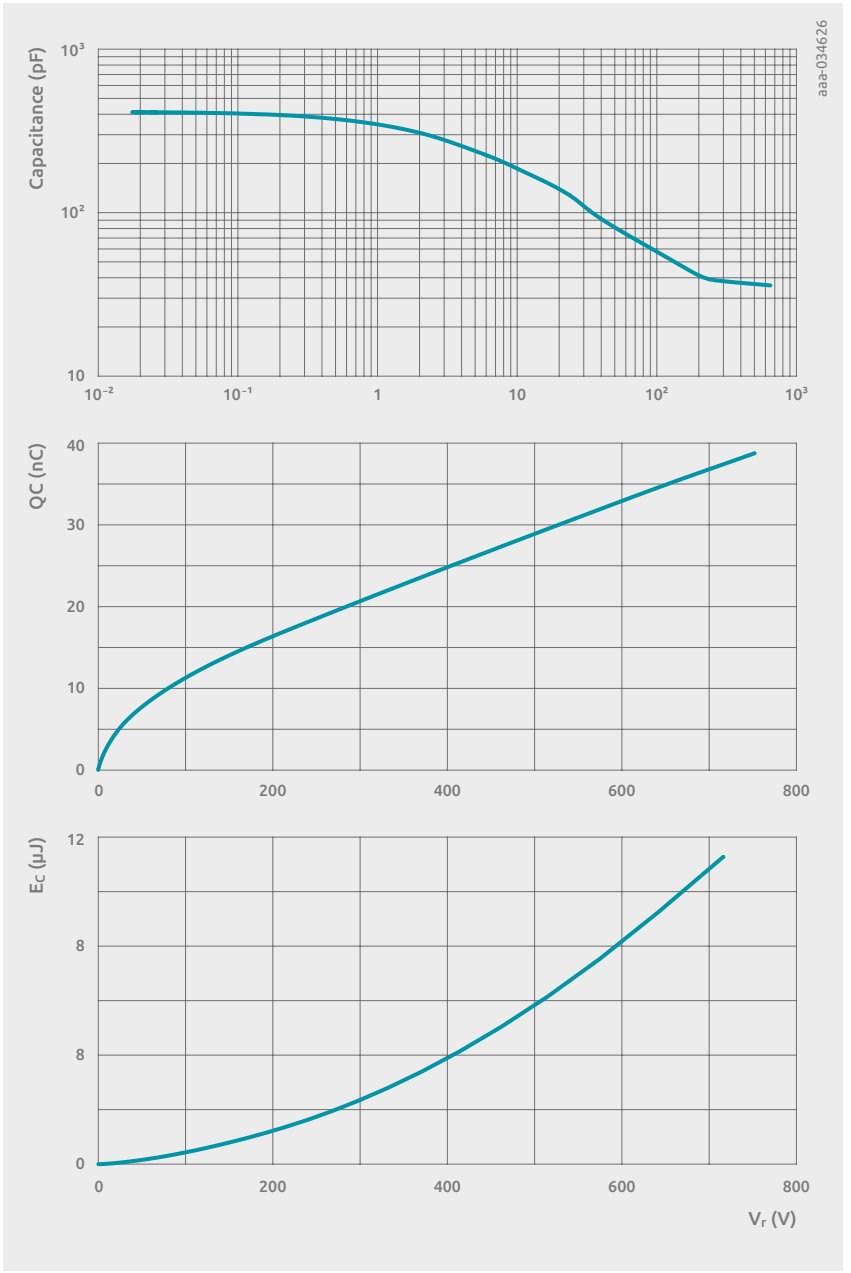


Figure 36 | Voltage dependency of the capacitive charge of SiC diodes and resulting stored energy.

2.6.4 Advanced SiC MPS process for maximum performance

As described earlier, the ratio between PN and Schottky area at a given die size determines the performance, both under nominal current and over-current conditions, and always leads to a trade-off between both aspects for a MPS diode. In order to further optimize these characteristics, more advanced process steps are required. One major influential parameter is the die thickness and its reduction for the final MPS design. The unprocessed silicon carbide substrate is n-doped. The epitaxial layers are subsequently grown on the SiC substrate. These substrates have a thicknesses of up to 500µm. Due to the doping concentration which is relatively low for SiC n-substrates, its influence on the total on-resistance of the processed diode is not negligible. As a consequence, both the voltage drop under normal operation as well as the over-current handling is adversely affected. As depicted in Figure 37, the thick substrate layer has no further electrical function but unfortunately acts as a series resistance through which the total current must flow.

To overcome this drawback, the underside of the substrate has to be thinned by grinding. However, due to the hardness of SiC (around 9.2 to 9.3 on the Mohs scale), grinding requires an advanced manufacturing process capability and precise control of the material quality. Inappropriate and inferior processes steps can lead to non-uniformities of die thickness or even die cracks, resulting in inferior performance or even device failures.

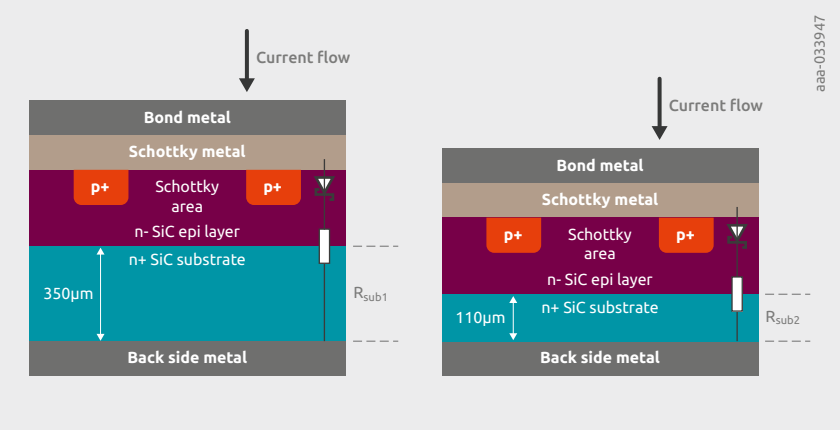


Figure 37 | Substrate resistance reduction through back-side grinding.

Nexperia's SiC MPS diodes are all ground down to a minimum thickness of substrate to maximize the diodes' performance without compromising mechanical stability.

Another positive aspect of the underside grinding refers to the thermal performance. As shown in Figure 38, the portion of the n-doped substrate on the thermal path is massively reduced.

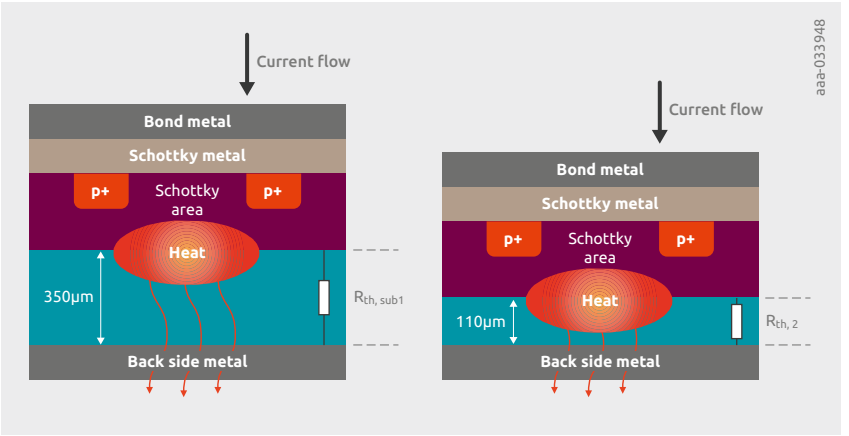


Figure 38 | Thermal improvement of Nexperia's backside optimized technology compared to a thick substrate solution.

When the diode has to dissipate heat, for example during forward conduction, the greater part of the heat flow is conducted through the diode's underside via the lead frame into the PCB. A thick substrate inserts not only an unnecessary electrical resistance, it also impacts the heat flow. Thus, it has negative impact on the maximum achievable performance and also the lifetime of the device. In contrast, using Nexperia's thin SiC technology massively improves the thermal performance. As a result, this leads to a lower thermal resistance, higher dissipated power and therefore higher power density. The surge current capability at given die size, in particular when the duration of such transient over-currents is comparably large, is also higher. Another consideration relates to the lifetime of the device. At a given power loss within a given application, the junction temperature swing is lower for the thinner device, leading to a longer lifetime and improved device reliability.

Although SiC diodes are already available in the market, there are still major differences in the ways various SiC manufacturers produce their parts. To enable designers to fully exploit the superior material properties of SiC versus Si, an advanced SiC design like the Merged PIN Schottky with optimized PN and Schottky ratio as well as quality and process control and special substrate handling is required. Nexperia has mastered all of these design and production steps to guarantee the maximum performance, highest reliability and best quality standards.

2.7 Zener diodes

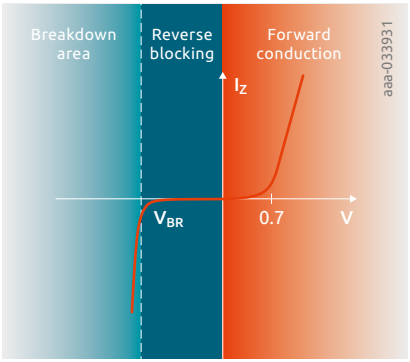
2.7.1 Introduction

When biased in the forward direction Zener diodes have the same characteristic as a silicon p-n diode. Most important for Zener diode applications is the characteristic when biased in the reverse direction, where Zener diodes have a small leakage current below a specific breakdown voltage. Above the breakdown voltage, the IV characteristic shows a steep increase of current. Zener diodes can operate constantly as voltage stabilizers at or above the breakdown voltage, V_Z.

These components are produced for many different voltages with guaranteed small ranges for V_Z tested at a defined reverse current I_Z. Figure 39 shows common symbols for a zener diode.

Figure 39 | Common symbols for a Zener diode.

Figure 40 shows the example of an IV curve of a zener diode. For positive voltages, the diode is in forward conduction. The current increases quite steeply if a voltage of about 0.7V is exceeded. In reverse direction, an area is depicted where the diode is blocking. Once the breakdown voltage is reached, current increases significantly. The voltage drop across the diode is kept almost constant in this area. An ideal Zener diode would keep V_Z constant independent on the current. In practice, bigger than zero. Zener diodes for voltages up to about 5V are realized with highly doped substrates. For such pn-diodes, an electrical breakdown happens if electrons can tunnel from the valence band into the conduction band across the depletion area of the reverse biased junction. The free charge carriers create a sudden increase in reverse current once the field strength is high enough. Clarence Melvin Zener discovered this effect in 1934 and gave his name to the resulting diodes. For Zener diodes with a breakdown voltage higher than 5V, a different breakdown effect becomes dominant. This is called the 'avalanche' breakdown and occurs when the electrical field across the pn-junction accelerates electrons in the transition area. These electrons create electron-hole pairs. Holes move to the negative electrode and get filled again, whereas the electrons move to the positive electrode. This motion of holes and electrons creates a leakage current through a negative biased diode. With high field strength, the mobile holes and electrons can generate more charge carriers by freeing up adjacent bound electrons. This process of generating more charge carriers creates an avalanche, causing a high current to flow once a specific reverse voltage is exceeded.



Both effects, zener and avalanche, are not distinguished when naming Zener diodes. No matter which physical effect dominates the breakdown of the pn-junction, all voltage reference diodes are referred to as Zener diodes.

Figure 40
I-V-characteristic of a Zener diode.

2.7.2 Datasheet parameters

Nexperia datasheets for Zener diodes start with a section 'General description'. The package type is given here. Datasheets for Zener diodes address the whole family of products including all working voltages. In the section 'Features and benefits', the working voltage range is mentioned. For Zener diodes that are offered with different tolerance selections of V_Z, is the nominal working voltage, this information is provided as well.

The chapter 'Quick reference data', as shown in Table 6, shows the maximum forward voltage V_F at a forward current I_F of 10mA for $T_{amb} = 25°C$. In order to avoid significant self-heating, this parameter is tested in pulsed mode.

The maximum total power dissipation P_{tot} is informed together with the description of the related mounting condition. Table 6 below is an example from the datasheet of BZX884S.

Table 6: 'Quick reference data' is an example from a Zener diode data sheet.

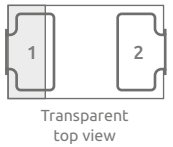
$T_j = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_F	forward voltage	$I_r = 10mA$	[1]	–	–	0,9	V
P_{tot}	total power dissipation		[2]	–	–	365	mW

[1] Pulse test: $t_p \leq 300\mu s$; $\delta \leq 0.02$
[2] Device mounted on a FR4 PCB, single sided 70µm copper, tin-plated and standard footprint.

Table 7 details the pinning of the diode. As for other diodes, the cathode is clearly marked with a bar in order to ensure correct mounting in the desired direction. Table 8 provides ordering information with type number, exact name, description and package style.

Table 7: Data sheet information regarding the pinning of an example Zener diode.

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode [1]	 Transparent top view	 006aaa152
2	A	anode		

[1] The marking bar indicates the cathode.

Table 8: Ordering information in the data sheet of an example Zener diode.

Type Number	Package		
	Name	Description	Version
BZX884S series [1]	DFN1006BD-2	Leadless ultra small plastic package with sidewettable flanks (SWF); 2 terminals; 0.65mm pitch; 1 × 0.6 × 0.47mm body	SOD882BD

[1] The series includes 37 breakdown voltages with nominal working voltages from 2.4V to 75V and ±2% and approximately ±5% tolerance.

The next datasheet section is named 'Marking' as illustrated in Table 9 . All available products with different working voltages in the two tolerance bands are listed together with the marking code. The name of later generation Zener diodes is simple to interpret. First, the Zener diode family name can be found. In the given example BZX884S. After this a character for tolerance is added. An indicator 'B' stands for 2% tolerance, the character 'C' for about 5%.

Nexperia introduced a bigger portfolio of zener diodes with an 'A' tolerance rating for the V_Z, which means 1% accuracy in order to address a growing demand for higher precision. Diodes in packages SOT23, SOD323 and SOD123F can be chosen.

After this, the working voltage follows, e.g. 2V4 for V_Z =2.4V. Integer voltage ratings show a number only and no V as separator.

Table 9: Section in the data sheet showing different working voltages with corresponding marking codes.

Type Number	Mark. Code	Type Number	Mark. Code	Type Number	Mark. Code
BZX884S-B2V4	2A	BZX884S-B27	3A	BZX884S-C8V2	5K
BZX884S-B2V7	2B	BZX884S-B30	3B	BZX884S-C9V1	5L
BZX884S-B3V0	2C	BZX884S-B33	3C	BZX884S-C10	3Y
BZX884S-B3V3	2D	BZX884S-B36	3D	BZX884S-C11	3Z
BZX884S-B3V6	2E	BZX884S-B39	3E	BZX884S-C12	4A
BZX884S-B3V9	2F	BZX884S-B43	3F	BZX884S-C13	4B
BZX884S-B4V3	2G	BZX884S-B47	3G	BZX884S-C15	4C
BZX884S-B4V7	2H	BZX884S-B51	3H	BZX884S-C16	4D
BZX884S-B5V1	2J	BZX884S-B56	3J	BZX884S-C18	4E
BZX884S-B5V6	2K	BZX884S-B62	3K	BZX884S-C20	4F
BZX884S-B6V2	2L	BZX884S-B68	3L	BZX884S-C22	4G
BZX884S-B6V8	N3	BZX884S-B75	3M	BZX884S-C24	4H
BZX884S-B7V5	2M	BZX884S-C2V4	4K	BZX884S-C27	4J
BZX884S-B8V2	2N	BZX884S-C2V7	4L	BZX884S-C30	4M
BZX884S-B9V1	2P	BZX884S-C3V0	4R	BZX884S-C33	4N
BZX884S-B10	2Q	BZX884S-C3V3	4S	BZX884S-C36	4P
BZX884S-B11	2R	BZX884S-C3V6	4T	BZX884S-C39	4Q
BZX884S-B12	2S	BZX884S-C3V9	4U	BZX884S-C43	4V
BZX884S-B13	2T	BZX884S-C4V3	4U	BZX884S-C47	4W
BZX884S-B15	2U	BZX884S-C4V7	4Y	BZX884S-C51	4Z
BZX884S-B16	2V	BZX884S-C5V1	5B	BZX884S-C56	5A
BZX884S-B18	2W	BZX884S-C5V6	5C	BZX884S-C62	5D
BZX884S-B20	2X	BZX884S-C6V2	5F	BZX884S-C68	5E
BZX884S-B22	2Y	BZX884S-C6V8	5G	BZX884S-C75	5H
BZX884S-B24	2Z	BZX884S-C7V5	5J	–	–

Table 10 contains the 'Limiting values'. The maximum forward current I_F is defined as well as the maximum total power dissipation P_{tot}, followed by the maximum junction temperature T_j and the allowed temperature ranges for ambient T_{amb} and storage T_{stg}.

Table 10: Specified limiting values in the data sheet of an example Zener diode.

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_F	forward current			–	200	mA
P_{tot}	total power dissipation	$T_{amb} = 25°C$	[1]	–	365	mW
T_j	junction temperature			–	150	°C
T_{amb}	ambient temperature			−55	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Device mounted on a FR4 PCB, single sided 70µm copper, tin-plated and standard footprint.

Table 11 details $R_{th(j-a)}$ for standard footprint on a single-sided PCB with 70 µm copper plating. This value could also be calculated with (150K–25K)/0.365W based on the limiting values given in Table 10.

Table 11: Definition of the junction to ambient thermal resistance in the data sheet of an example Zener diode.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	–	–	340	K/W

[1] Device mounted on a FR4 PCB, single sided 70µm copper, tin-plated and standard footprint.

In Table 12 showing 'characteristics', the maximum forward voltage drop at I_F of 10mA is informed, as in Table 6.

Table 12: Section "characteristics" in the data sheet of an example Zener diode.

$T_j = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_F	forward voltage	$I_r = 10mA$	[1]	–	–	0,9	V

[1] Pulse test: $t_p \leq 300µs$; $\delta \leq 0.02$

The three tables summarized in Table 13 list several very important parameters of the diodes. First column is the name extension, followed by a column for the accuracy ranges provided per diode. The third column provides minimum and maximum V_Z values for a reverse current of 5mA. When V_Z equals or exceeds 27V the testing current is reduced. An I_Z of 2mA instead of 5mA is applied because power dissipation would become quite high with $P = V_Z * I_Z$ in case of a high breakdown voltage. Additional operating cases are tested in mass production to ensure that the whole V_Z-I_Z curve is correct in the reverse blocking area as well as in forward conduction and in breakdown area.

The differential resistance is defined as $r_{dif} = \frac{\Delta V_Z}{\Delta I_Z}$ and listed in the fourth column. This is the steepness of the V_Z-I_Z curve. The ideal would be a dynamic resistance of 0 ohms or a perpendicular curve. In this case, V_Z would not change with reverse current and the breakdown voltage would stay stable, independent of the current applied.

The fifth column lists the maximum reverse or leakage current at about 2/3 of V_{BR}. The next column contains the thermal coefficient S_Z in mV/K valid for an I_Z of 5mA. The breakdown voltage is dependent on the junction temperature and can be calculated with the simple formula below:

$$V_Z = V_{Z(nominal)} + S_Z \times (T_j - 25°C)$$

For low voltage zener diodes, S_Z is a negative coefficient, so V_Z decreases over temperature. The breakdown mechanism is the Zener effect. Above about 6V, the sign of S_Z changes and the avalanche effect becomes dominant.

Finally there is a column for the diode capacitance Cd tested at $V_R = 0V$ and $f = 1MHz$.

Table 13: Characteristics per type

BZX884S-B2V4 to BZX884S-C24

$T_j = 25°C$ unless otherwise specified

BZX884S	Sel	Working voltage V_Z (V)		Differential resistance r_{dif} (Ω)				Reverse current I_R (μA)		Temperature coefficient S_Z (mV/K)		Diode capacitance C_d (pF) [1]
		I_Z = 5mA		I_Z = 1mA		I_Z = 5mA				I_Z = 5mA		
		Min	Max	Typ	Max	Typ	Max	Max	V_R (V)	Min	Max	Max
2V4	B	2.35	2.45	275	600	70	100	50	1.0	−3.5	0.0	260
	C	2.20	2.60									
2V7	B	2.65	2.75	300	600	75	100	20	1.0	−3.5	0.0	260
	C	2.50	2.90									
3V0	B	2.94	3.06	325	600	80	95	10	1.0	−3.5	0.0	260
	C	2.80	3.20									
3V3	B	3.23	3.37	350	600	85	95	5	1.0	−3.5	0.0	260
	C	3.10	3.50									
3V6	B	3.53	3.67	375	600	85	90	5	1.0	−3.5	0.0	260
	C	3.40	3.80									
3V9	B	3.82	3.98	400	600	85	90	3	1.0	−3.5	0.0	260
	C	3.70	4.10									
4V3	B	4.21	4.39	410	600	80	90	3	1.0	−3.5	0.0	260
	C	4.00	4.60									
4V7	B	4.61	4.79	425	500	50	80	3	2.0	−3.5	0.2	170
	C	4.40	5.00									
5V1	B	5.00	5.20	400	480	40	60	2	2.0	−2.7	1.2	170
	C	4.80	5.40									
5V6	B	5.49	5.71	80	400	15	40	1	2.0	−2.0	2.5	170
	C	5.20	6.00									
6V2	B	6.08	6.32	40	150	6	10	3	4.0	0.4	3.7	120
	C	5.80	6.60									
6V8	B	6.66	6.94	30	80	6	15	2	4.0	1.2	4.5	120
	C	6.40	7.20									

[1] f = 1MHz; V_R = 0V

$T_j = 25°C$ unless otherwise specified

BZX884S	Sel	Working voltage V_Z (V)		Differential resistance r_{dif} (Ω)				Reverse current I_R (μA)		Temperature coefficient S_Z (mV/K)		Diode capacitance C_d (pF) [1]
		I_Z = 5mA		I_Z = 1mA		I_Z = 5mA				I_Z = 5mA		
		Min	Max	Typ	Max	Typ	Max	Max	V_R (V)	Min	Max	Max
7V5	B	7.35	7.65	30	80	6	15	1	5.0	2.5	5.3	150
	C	7.00	7.90									
8V2	B	8.04	8.36	40	80	6	15	0.7	5.0	3.2	6.2	150
	C	7.70	8.70									
9V1	B	8.92	9.28	40	100	6	15	0.5	6.0	3.8	7.0	150
	C	8.50	9.60									
10	B	9.80	10.20	50	150	8	20	0.2	7.0	4.5	8.0	90
	C	9.40	10.60									
11	B	10.80	11.20	50	150	10	20	0.1	8.0	5.4	9.0	85
	C	10.40	11.60									
12	B	11.80	12.20	50	150	10	25	0.1	8.0	6.0	10.0	85
	C	11.40	12.70									
13	B	12.70	13.30	50	170	10	30	0.1	8.0	7.0	11.0	80
	C	12.40	14.10									
15	B	14.70	15.30	50	200	10	30	0.05	10.5	9.2	13.0	75
	C	13.80	15.60									
16	B	15.70	16.30	50	200	10	40	0.05	11.2	10.4	14.0	75
	C	15.30	17.10									
18	B	17.60	18.40	50	225	10	45	0.05	12.6	12.4	16.0	70
	C	16.80	19.10									
20	B	19.60	20.40	60	225	15	55	0.05	14.0	14.4	18.0	60
	C	18.80	21.20									
22	B	21.60	22.40	60	250	20	55	0.05	15.4	16.4	20.0	60
	C	20.80	23.30									
24	B	23.50	24.50	60	250	25	70	0.05	16.8	18.4	22.0	55
	C	22.80	25.60									

[1] f = 1MHz; V_R = 0V

BZX884S-B27 to BZX884S-C75

$T_j = 25°C$ unless otherwise specified

BZX884S	Sel	Working voltage V_Z (V)		Differential resistance r_{dif} (Ω)				Reverse current I_R (μA)		Temperature coefficient S_Z (mV/K)		Diode capacitance C_d (pF) [1]
		I_Z = 2mA		I_Z = 0.5mA		I_Z = 2mA				I_Z = 2mA		
		Min	Max	Typ	Max	Typ	Max	Max	V_R (V)	Min	Max	Max
27	B	26.50	27.50	65	300	25	80	0.05	18.9	21.4	25.3	50
	C	25.10	28.90									
30	B	29.40	30.60	70	300	30	80	0.05	21.0	24.4	29.4	50
	C	28.00	32.00									
33	B	32.30	33.70	75	325	35	80	0.05	23.1	27.4	33.4	45
	C	31.00	35.00									
36	B	35.30	36.70	80	350	35	90	0.05	25.2	30.4	37.4	45
	C	34.00	38.00									
39	B	38.20	39.80	80	350	40	130	0.05	27.3	33.4	41.2	45
	C	37.00	41.00									
43	B	42.10	43.90	85	375	45	150	0.05	30.1	37.6	46.6	40
	C	40.00	46.00									
47	B	46.10	47.90	85	375	50	170	0.05	32.9	42	51.8	40
	C	44.00	50.00									
51	B	50.00	52.00	90	400	60	180	0.05	35.7	46.6	57.2	40
	C	48.00	54.00									
56	B	54.90	57.10	100	425	70	200	0.05	39.2	52.2	63.8	40
	C	52.00	60.00									
62	B	60.80	63.20	120	450	80	215	0.05	43.4	58.8	71.6	35
	C	58.00	66.00									
68	B	66.60	69.40	150	475	90	240	0.05	47.6	65.6	79.8	35
	C	64.00	72.00									
75	B	73.50	76.50	170	500	95	255	0.05	52.5	73.4	88.6	35
	C	70.00	79.00									

[1] $f = 1MHz$; $V_R = 0V$

Figure 41 shows the I-V-curve of diode BZX884S-B/C6V8 for forward direction with a logarithmic scale for I_F.

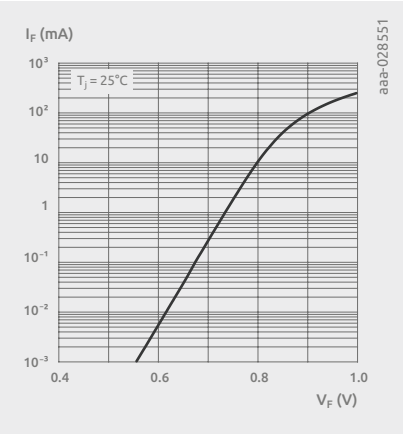


Figure 41 | Forward current as a function of forward voltage; typical values BZX884S-B/C6V8-Q.

Figure 42 depicts how the temperature coefficient S_Z varies over the working current I_Z. For lower working voltages there is a quite significant influence on this coefficient. From Figure 43 it can be concluded that S_Z becomes almost constant over I_Z for working voltages above 7.5V.

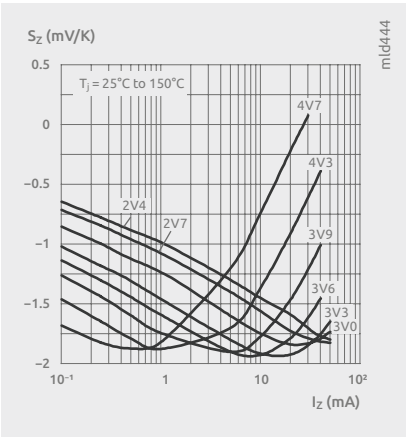


Figure 42 | Temperature coefficient as a function of working current; typical values BZX884S-B/C2V4-Q to B/C4V7-Q.

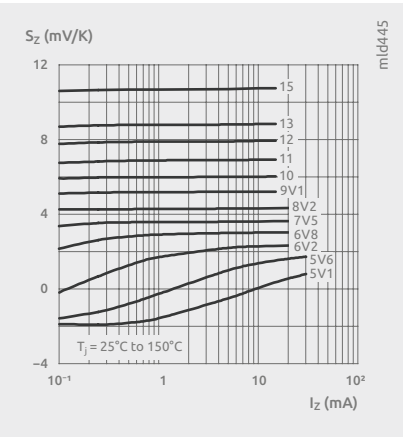


Figure 43 | Temperature coefficient as a function of working current; typical values BZX884S-B/C5V1-Q to B/C15-Q.

For Zener diodes the I-V characteristic in reverse direction shows how effectively the component can be used to stabilize a voltage. For low Zener voltages, the breakdown voltage increases significantly versus reverse current as shown in Figure 44. In this diagram the reverse direction I-V-curves from 2.4 V up to 6.8 V are depicted. Figure 45 and Figure 46 show the reverse direction characteristics for higher voltage Zener diodes from the BZX884S series. These devices get quite close to an ideal Zener diode which would have a perpendicular I-V characteristic at the nominal V_Z voltage, so reverse current I_Z would not have an impact on the breakdown voltage.

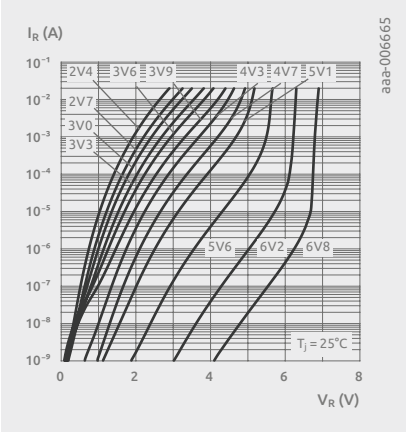


Figure 44 | Reverse current as a function reverse voltage; typical values (BZX884S-B/C2V4-Q to B/C6V8-Q.

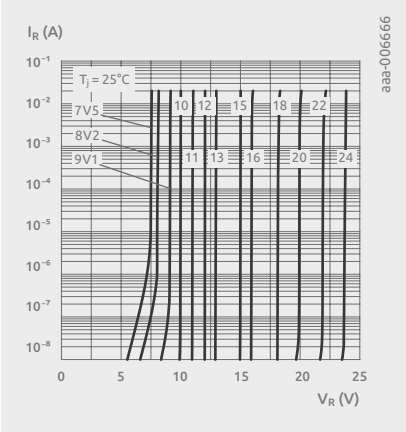


Figure 45 | Reverse current as a function reverse voltage; typical values (BZX884S-B/C7V5-Q to B/C24-Q.

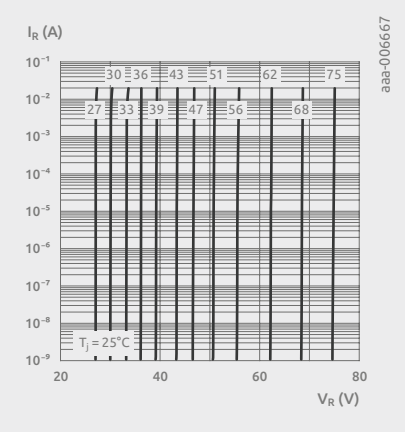


Figure 46 | Reverse current as a function reverse voltage; typical values (BZX884S-B/C27-Q to B/C75-Q.

2.7.3 Zener diodes package overview

Nexperia offers zener diodes in a wide range of packages. Table 14 shows all options from small DFN1006 packages up to the bigger variants like SOT223 with increasingly higher power capability.

The values in column 3 apply for mounting the devices on an FR4 PCB with a standard footprint. The board uses single-sided copper with tin-plating.

Table 14: Nexperia's packages for zener diodes, configuration and P_{tot} ratings.

Package name	configuration	P_{tot} (mW)
DFN1006BD-2 (SOD882BD)	single	365
DFN1006(D)-2 (SOD882)	single	250
SOD523	single	300
SOD323	single	300/400/490
SOD323F	single	310
SOT23	single, dual	250/300
SOT323	Single, dual	250/275/300/350
SOD123	single	365/590
SOD123F	single	500/830
SOT89	single	1000
SOT223	single	1500
SOD80C (MiniMelf)	single	500
SOD27 (DO-35)	single	500
SOD66 (DO-41)	single	1000/1300

Chapter 3

Data sheet parameters

3.1 Introduction

In the course of selecting the most suitable diode for any application there is no way around taking a look into the datasheet. This selection process needs to be carried out with a lot of care since different semiconductor manufacturers specify the same parameter under different conditions, making two different products hard to compare. Knowing this already highlights that understanding datasheet parameters is key to successful application design.

The objective of this chapter is to provide engineers with an efficient path through a Nexperia diode datasheet and highlight special application and technology related parameters. We have taken as our example the PMEG45T20EXD-Q datasheet. The PMEG45T20EXD-Q is an 45V 2A trench MEGA (maximum efficiency general application) automotive qualified (according to AEC-Q101) Schottky barrier rectifier. In this case 45V is the reverse blocking voltage and 2A the average DC forward current.

3.2 Understanding Nexperia datasheet parameters and where they can be found

Since Nexperia offers a wide portfolio of diodes, sections of special diode products can deviate from the generic structure. Nevertheless, the following subsection is representative of the general datasheet structure for Nexperia diodes. Datasheets for zener diodes address a complete diode family not a single product only. Therefore they include a special subsection with a table specific parameters like breakdown voltages V_Z, thermal coefficient of V_Z and others.

3.2.1 Quick reference data

Section 4 in the datasheet is a good early indicator of whether a particular diode is suitable for the target application. In the 'Quick reference data' section the most important electrical characteristics of the device are summarized in the table. Table 15 shows the excerpt from the respective section of the PMEG45T20EXD-Q datasheet.

Table 15: Example: Quick reference data out of the PMEG45T20EXD-Q datasheet.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{F(AV)}$	average forward current	$\delta = 0.5$; $f = 20kHz$; square wave; $T_{sp} \leq 166°C$		–	–	2	A
V_R	reverse voltage	$T_j = 25°C$		–	–	45	V
V_F	forward voltage	$I_F = 2A$; pulsed; $T_j = 25°C$	[1]	–	500	560	mV
I_R	reverse current	$V_R = 45V$; pulsed; $T_j = 25°C$	[1]	–	4	25	µA
		$V_R = 45V$; pulsed; $T_j = 125°C$	[1]	–	3	9	mA

[1] Very short pulse, in order to maintain a stable junction temperature.

The average forward current $I_{F(AV)}$ of the diode specifies the current capability for a specific waveform without damage occurring through overheating. When comparing multiple $I_{F(AV)}$ ratings, special attention must paid to the measurement conditions. Nexperia specifies $I_{F(AV)}$ for a 20kHz square wave with a 50% duty cycle δ. The duty cycle definition is given in Figure 47. For a δ of 0.5 and a switching frequency f of 20kHz $t_2 = \frac{1}{20kHz} = 50µs$ and $t_1 = t_2 \cdot \delta = 25µs$.

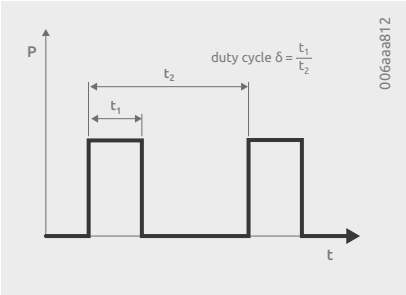


Figure 47 | Duty cycle definition. Nexperia specifies $I_{F(AV)}$ for a 20kHz square wave with a 50% duty cycle.

The current ratings for the typical waveforms can be obtained using following equations:

$$I_{F(AV)} = I_M \cdot \delta$$

$$I_{RMS} = I_{F(AV)} \text{ at } DC \& I_{RMS} = I_M \cdot \sqrt{\delta}$$

Here I_M is defined as peak current and I_{RMS} as the root mean square current (RMS). At DC, I_{RMS} equals the average current. In other words the I_{RMS} value gives the same heating effect as $I_{F(AV)}$ for DC condition or any other DC current of same value. Some vendors specify the $I_{F(AV)}$ using positive 60Hz half sine waves. Calculating the average power for both current waveforms over two periods of the half sine wave leads to the result that the average power in the square wave is roughly the same order of magnitude as the sine half wave itself.

Please note: the $I_{F(AV)}$ rating is specified according to a maximum solder point temperature. In this case it is 166°C.

The next value in the 'Quick reference data' table is the reverse blocking voltage V_R. This determines the maximum allowable reverse voltage the diode is able to withstand before entering breakdown operation, which usually leads to destruction of the part. The reverse blocking voltage alongside the average current are the key parameters used in the naming convention of Nexperia diodes. Thus the PMEG45T20EXD-Q has a V_R of 45V and a maximum $I_{F(AV)}$ of 2A. As mentioned in sub-section 1.3, both forward and reverse characteristics exhibit a strong temperature dependency. Thus when discussing the forward voltage and the leakage current in the 'Quick reference data section' it should be highlighted that these two values are measured using a very short pulse at room temperature (footnote 1 in Table 15) to avoid self-heating . The forward voltage drop of a diode, V_F, determines conduction loss of the diode when it is forward biased. This is very important in high efficiency applications like SMPS, or for reverse polarity protection. Here, V_F should be kept as low as possible. The last value in the 'Quick reference table' is the reverse current I_R, also known as the leakage current. This is the amount of current which will pass through the diode when it is reverse biased. With reverse power $P_R = V_R \times I_R$, the leakage current I_R defines how much power is generated in reserve direction for a given reverse voltage.

3.2.2 Pinning-, ordering- and marking information

After the most relevant technical parameters have been discussed, sections 5–7 cover product specific information, such as ordering code and markings, as can be seen in Table 16. Here the transparent top view in the simplified outline column is a great help when employing the device during the prototyping phase while using manual assembly.

Table 16: Pinning information of the PMEG45T20EXD-Q.

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 Transparent top view CFP2-HP (SOD323HP)	 sym001
2	A	anode		

The Ordering Information table (Table 17) contains a unique type number. This gains more importance if a die is available in multiple packages. If that is the case, the last letter (for newer packages the last two letters) is the package designator. Besides the type number, the package name, body dimension and version is given.

Table 17: Ordering information PMEG45T20EXD-Q.

Type Number	Package		
	Name	Description	Version
PMEG45T20EXD-Q	CFP2-HP	SOD323HP: plastic surface-mounted package with solderable lead ends; 2.2 × 1.3 × 0.68mm body	SOD323HP

3.2.3 Limiting values

Section 8 is the most crucial section of the datasheet and should be studied with great care before operating the device. The limiting values state the specified absolute maximum ratings that the device can operate to. These values are guaranteed by Nexperia and in are accordance to the 'Absolute Maximum rating System' (IEC60134). Stresses beyond those levels or any other condition is not recommended or guaranteed. Exposure to absolute maximum ratings for extended periods of times may also have an influence on device functionality. The limiting values for the PMEG45T20EXD-Q are depicted in Table 18.

Table 18: Limiting values PMEG45T20EXD-Q.

Symbol	Parameter	Conditions		Min	Max	Unit
V_R	reverse voltage	$T_j = 25°C$		–	45	V
I_F	forward current	$\delta = 1$; $T_{sp} \leq 165°C$		–	2.8	A
$I_{F(AV)}$	average forward current	$\delta = 0.5$; $f = 20kHz$; square wave; $T_{sp} \leq 166°C$		–	2	A
I_{FSM}	non-repetitive peak forward current	$t_p = 8.3ms$; half sine wave; $T_{j(init)} = 25°C$		–	22	A
P_{tot}	total power dissipation	$T_{amb} \leq 25°C$	[1]	–	0.65	W
			[2]	–	1.2	W
T_j	junction temperature			–	175	°C
T_{amb}	ambient temperature			−55	175	°C
T_{stg}	storage temperature			−65	175	°C

[1] Device mounted on a FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated and standard footprint.
[2] Device mounted on a FR4 PCB, single sided copper, tin-plated mounting pad for cathode 1cm².

The reverse voltage V_R and the average forward current $I_{F(AV)}$ have already been discussed in the 'Quick reference data' section. In comparison to $I_{F(AV)}$, the forward current IF states the maximum constant current allowed for a duty cycle operation of 1 – in other words, DC conditions. Here, solder point temperature has been kept below 165°C. Contrary to I_F, the non-repetitive peak forward current I_{FSM} specifies the maximum allowed single current pulse. Hence I_{FSM} is a measure for the surge current capability of a diode. It is important to notice that I_{FSM} is valid for single events, like inrush currents at start-up or in load dump scenarios, only. The test pulse used to characterize this is a single cycle, half sine wave with a pulse length tp of 8.3ms which corresponds to 60Hz half sine wave. This pulse has historical background since diodes where originally used to rectify 50/60Hz main from AC to DC. The current pulse is depicted in Figure 48 for a diode which has an I_{FSM} value of 50A.

Figure 48 | I_{FSM} measurement: half sine wave with a pulse width of 8.3ms for a clip bonded diode.

Experience has shown that the I_{FSM} capability of a device will already vary significantly when comparing two devices in the same package with different active chip areas (Figure 49) or bonding technologies (Figure 50). Even mounting conditions have an impact on I_{FSM}.

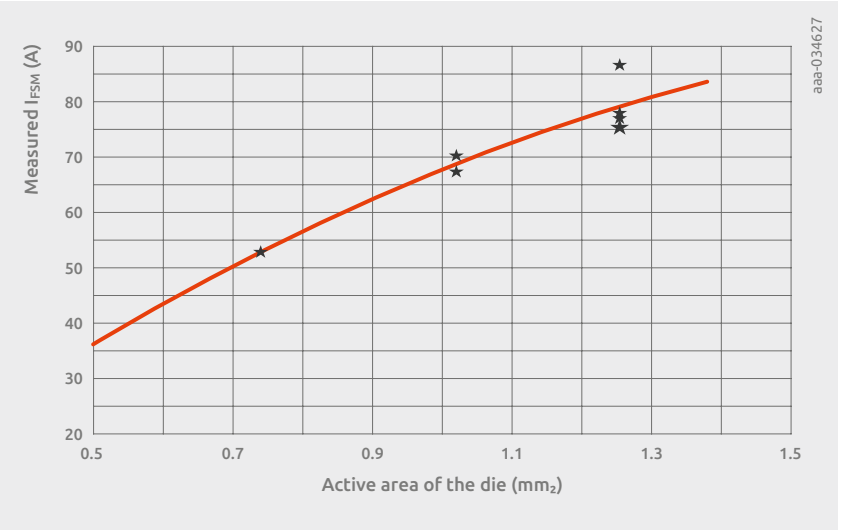


Figure 49 | I_{FSM} for a 5.5ms square wave pulse as a function of active chip area.

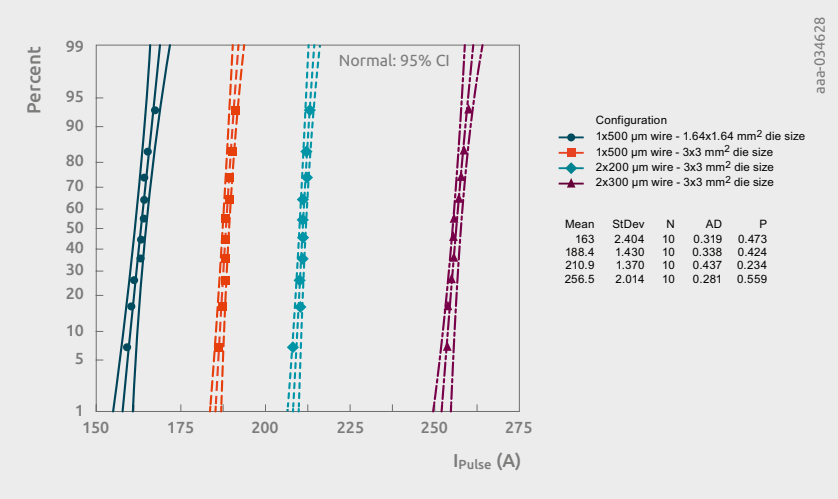


Figure 50 | Probability Plot of D²PAK for different Bonding technologies.

Also, trying to approximate I_{FSM} for different pulse length is not that simple since there is no fully linear relationship. It can be stated that I_{FSM} increases for short pulse durations, if the junction temperature does not exceed the silicon limit, and vice versa. For long pulse duration the power dissipating capabilities of the package and the connection to the solder point contributes to the I_{FSM} capability compared to short pulse durations. Here, all generated heat needs to be dissipated in the junction itself. The initial junction temperature when measuring I_{FSM} $T_{j(init)}$ is 25°C. The device junction heats up to a high temperature while experiencing the test pulse, therefore the I_{FSM} value will degrade fast for $T_{j(init)}$ above 25°C.

The total power dissipation, P_{tot}, is the maximum allowable power the diode is able to dissipate during steady state operation while not exceeding the maximum allowable junction temperature, in this case 175°C. During measurement, the ambient temperature is controlled to be equal or less than 25°C. P_{tot} depends greatly on the mounting conditions as can be seen in case of the PMEG45T20EXD-Q in Table 18. Here, there are two P_{tot} values stated. The first one is for standard footprint on the PCB as in Nexperia's footprint recommendation at the end of the datasheet. Here no optimal heat spread into the PCB is provided and thus the benefits of CFP2-HP package cannot be fully used. This is different for the second P_{tot} value in the table. This power is meant for a 1cm² heat sink which is located at the cathode tab. This condition is thermally comparable to a four-layer PCB and enables the PMEG45T20EXD-Q to dissipate nearly twice as much continuous power compared to the standard footprint. For ease of visualization, both layout variants are depicted in Figure 51.

Figure 51 | Example CFP2-HP test boards: 1cm² mounting pad for cathode vs. standard footprint.

The maximum junction temperature T_J dictates the temperature limit of the die. Violating this limit may damage the diode irreversibly, as exceeding any of the other limiting values would also do. The maximum ambient T_{amb} is typically equal to the maximum T_J. The same is true for the storage temperature T_{stg}. The minimum and maximum T_{amb} indicates the temperature environment that the device can be in while complying with the other datasheet parameters. T_{stg} sets the temperature range in which the device can be stored without affecting its reliability. For long term storage, an inert atmosphere will prohibit device degradation.

3.2.4 Thermal characteristics

This sub-section of the datasheet provides information about the thermal behavior of the device, considering different reference points and conditions. The thermal resistance R_{th} is the steady-state parameter of how much the device will heat up for a constant power flow under DC conditions. Hence the unit is Kelvin per Watt. In other datasheets this is sometimes expressed as Celsius per Watt. Since the thermal resistance describes temperature difference, both are the same. The subscript j-x states temperature difference from junction point of view to a specific reference point. A high-level visualization of prominent heat paths is shown on the cross section of typical clip bonded package depicted in Figure 52.

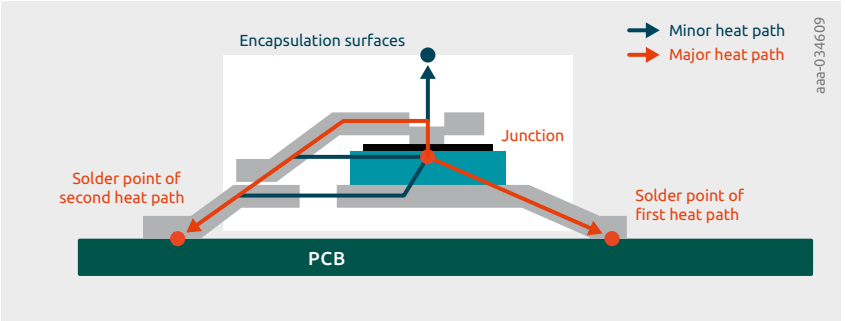


Figure 52 | Cross section of a typical clip bonded flat power package – heat paths highlighted.

Nexperia uses two different thermal resistances to specify the thermal characteristics of its devices. The first value is the thermal resistance from the junction to ambient and can be identified by the index (j-a). The second value is from junction to the solder point of the cathode tab (indicated as "first heat path" in Figure 52) and has the index (j-sp). For completeness, the minor thermal heat path from junction to the topside of the case is also indicated in Figure 52. This heat path might be prominent if topside cooling is to be considered. Some Nexperia packages such as CCPAK12 support topside cooling. The main heat path for SMD components is from junction to solder point into the PCB. For comparing packages from different vendors by using $R_{th(j-a)}$ it is very important to also check the parameters like PCB type and footprint which have a huge impact on the $R_{th(j-a)}$. The thermal characteristics for the PMEG45T20EXD-Q under DC conditions are shown in Table 19.

Table 19: Thermal characteristics of the PMEG45T20EXD-Q.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	–	–	230	K/W
			[1] [3]	–	–	125	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		[4]	–	–	6	K/W

[1] For Schottky barrier diodes thermal runaway has to be considered, as in some applications the reverse power losses P_R are a significant part of the total power losses.
[2] Device mounted on a FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated and standard footprint.
[3] Device mounted on a FR4 PCB, single sided copper, tin-plated mounting pad for cathode 1cm².
[4] Soldering point of cathode tab.

Nexperia specifies the thermal resistance from the junction to the ambient $R_{th(j-a)}$ for two different mounting conditions. The first value is valid for the use of standard footprint. It delivers the highest thermal resistance since the diode has a limited heat path. The diode will heat up faster for the same amount of dissipated power compared to the second value which uses a 1cm² heat sink for the cathode. As mentioned by footnote 1 in Table 19, when the reverse power losses generated within the diode due to leakage current exceed the power dissipated by the

package, the diode can fail. This is called 'thermal runaway' and will be explained in more detail in chapter 3.3. To avoid this, the following formula should be adhered to:

$$\frac{\delta P_{diss}}{\delta T_J} < \frac{1}{R_{th(j-a)}}$$

Figure 53 shows the comparison of thermal plots for a standard footprint layout and one using a 1cm² heat sink with the PMEG45T20EXD at a continuous power dissipation of 1.07W, using infrared camera measurement. The temperature difference in thermal equilibrium is greater than 30°C. Note the infrared camera only captures the topside temperature. The actual junction temperature is higher.

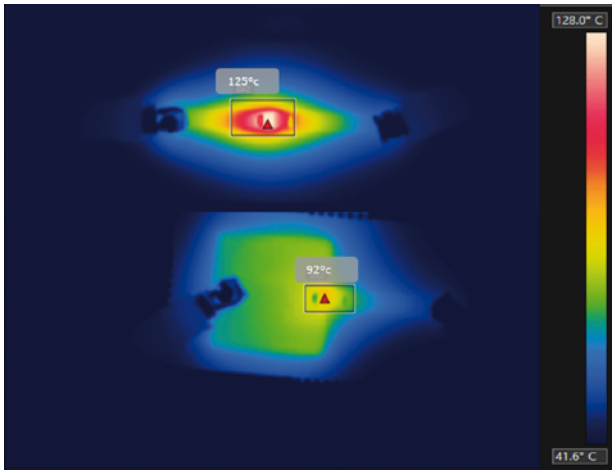


Figure 53
Comparison of infrared camera measurements of PMEG45T20EXD-Q on standard footprint (top) and on footprint with 1cm² heatsink at 1.07W continuous power dissipation.

The $R_{th(j-sp)}$ in Table 19 characterizes the heat transfer from the junction through the leadframe up to the solder point of the cathode tab. Therefore it is not influenced by the type of PCB or the kind of footprint. This is the reason why no definition of the mounting condition is needed for this parameter. As R_{th} describes the steady state operation, the thermal impedance Z_{th} represents the dynamic thermal behavior. Since $Z_{th(j-x)}$ is a dynamic parameter, it is shown in the curves as a function of pulse duration for different duty cycles. For duty cycle definition please refer to Figure 47. A duty cycle of 0 equals single pulse operation and a duty cycle of 1 indicates DC operation. Figure 54 shows an array of $Z_{th(j-a)}$ curves as a function of pulse duration and duty cycle for PMEG45T20EXD-Q.

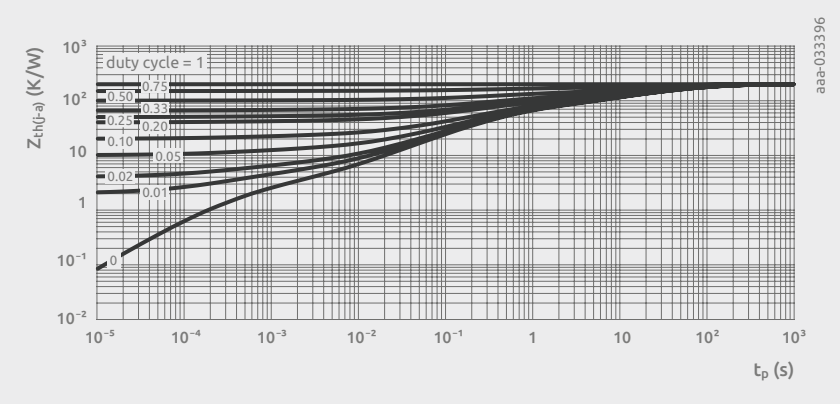


Figure 54 | $Z_{th(j-a)}$ as a function of pulse duration and duty cycle for PMEG45T20EXD-Q; typical values.

The key information given by these curves is that the device can sustain more power for small duty cycles or short pulse duration. The rise of junction temperature for a given power dissipation can be calculated via equation:

$$\Delta T = | Z_{th(j-x)} | \cdot P_{diss}$$

Where P_{diss} is the dissipated power by the diode. $Z_{th(j-x)}$ indicates how the device responds to transient thermal events and converges to the thermal resistance R_{th} for long pulse duration. For the steady state the above equation can be written as:

$$\Delta T = | R_{th(j-x)} | \cdot P_{diss}$$

For a more detailed derivation of the thermal resistance please refer to chapter 4.

3.2.5 Electrical characteristics

The complete electrical characteristics of the diode are provided in section 10 of the datasheet. The reverse and forward parameters stated here are measured using very short pulses to avoid self-heating of the device.

Table 20: Datasheet characteristics of the PMEG45T20EXD-Q.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)B}$	reverse break-down voltage	I_R = 1mA; pulsed; T_j = 25°C	[1]	45	–	–	V
V_F	forward voltage	I_F = 0.1A; pulsed; T_j = 25°C	[1]	–	330	385	mV
		I_F = 0.5A; pulsed; T_j = 25°C	[1]	–	390	445	mV
		I_F = 0.7A; pulsed; T_j = 25°C	[1]	–	410	465	mV
		I_F = 1A; pulsed; T_j = 25°C	[1]	–	430	490	mV
		I_F = 2A; pulsed; T_j = 25°C	[1]	–	500	560	mV
		I_F = 2A; pulsed; T_j = −40°C	[1]	–	540	600	mV
		I_F = 2A; pulsed; T_j = 125°C	[1]	–	440	500	mV
		I_F = 2A; pulsed; T_j = 150°C	[1]	–	430	490	mV
I_R	reverse current	V_R = 10V; pulsed; T_j = 25°C	[1]	–	2	10	µA
		V_R = 45V; pulsed; T_j = 25°C	[1]	–	4	25	µA
		V_R = 45V; pulsed; T_j = 125°C	[1]	–	3	9	mA
		V_R = 45V; pulsed; T_j = 150°C	[1]	–	11	40	mA
C_D	diode capacity	V_R = 4V; f = 1MHz; T_j = 25°C		–	160	–	pF
		V_R = 10V; f = 1MHz; T_j = 25°C		–	100	–	pF
t_{rr}	reverse recovery time step recovery	I_F = 0.5A; I_R = 1A; $I_{R(meas)}$ = 0.25A; T_j = 25°C		–	5	–	ns
	reverse recovery time ramp recovery	dI_F/dt = 100A/µs; I_F = 1A; V_R = 30V, T_j = 25°C		–	9	–	ns
I_{RM}	peak reverse recovery current	dI_F/dt = 100A/µs; I_F = 1A; V_R = 30V, T_j = 25°C		–	0.38	–	A
Q_{RR}	reverse recovery charge	dI_F/dt = 100A/µs; I_F = 1A; V_R = 30V, T_j = 25°C		–	2.5	–	nC
V_{FRM}	peak forward recovery voltage	I_F = 0.5A; dI_F/dt = 20A/µs; T_j = 25°C		–	405	–	mV

[1] Very short pulse, in order to maintain a stable junction temperature.

As described in chapter 1, diodes can be operated in three different states. To enter breakdown operation, the reverse voltage must be greater than or equal to the reverse breakdown voltage $V_{(BR)R}$. The forward voltage drop V_F has already been introduced in the section discussing the quick reference data. In Table 20 V_F is given for different operating points and junction temperatures. For a more detailed representation of the forward characteristics, the forward current as a function of forward voltage should be studied, as illustrated in Figure 55. These curves are given for the complete temperature range of the device and allow the user to estimate device performance under different conditions.

As for the forward characteristics, the reverse characteristics are stated for different operating points. As already mentioned in the quick reference section, for the PMEG45T20EXD-Q the reverse current increases by three orders of magnitude for a temperature difference of 100°C. If the temperature is kept constant and V_R is reduced by factor of 4, I_R reduces by a factor of two only. Figure 56 depicts the reverse current as a function of reverse voltage for different temperatures.

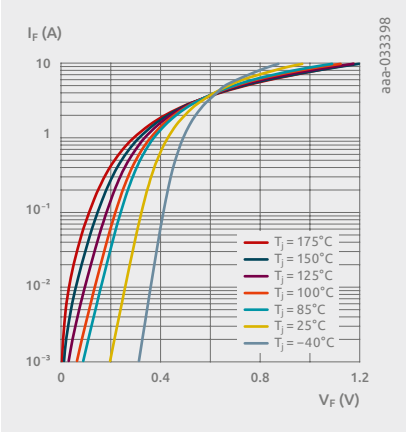


Figure 55 | Forward current as a function of forward voltage; typical values PMEG45T20EXD-Q.

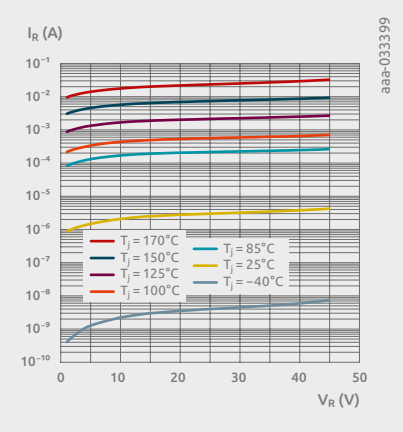


Figure 56 | Reverse current as a funtion of reverse voltage and temperature; PMEG45T20EXD-Q.

The following parameters describe the transient response of the diode. Due to the nature of the junction, any variation in applied voltage will cause a change for the number of charge carriers. If the voltage is applied in reverse direction, electric charge is stored at the depletion region. This charge is then acting like a parallel plate capacitor. The resulting capacitance is called junction capacitance C_D and is directly linked to the change in charge for a given voltage change by $C_D = \frac{dQ}{dV_R}$. The junction capacitance is also called transition capacitance and therefore denoted as C_T in datasheets of other vendors. Since the junction capacitance generally varies not only with voltage but also with frequency, C_D is specified at a dedicated frequency. Many manufacturers, including Nexperia, specify C_D at 1MHz and provide it as function of reverse voltage as can be seen in Figure 57. The capacitance C_D decreases with increasing reverse voltage.

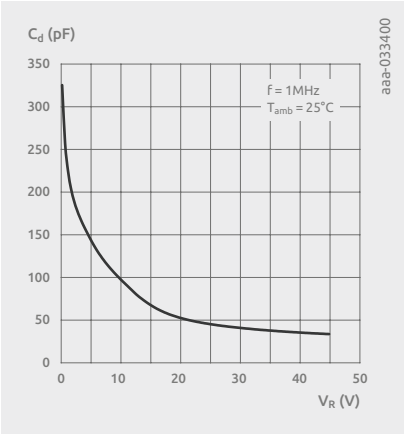


Figure 57 | Diode capacitance as a function of reverse; PMEG45T20EXD-Q.

The time required by the device to establish full blocking capability after one current commutation is called reverse recovery time t_{rr}. Nexperia provides two reverse recovery times. One for step response as shown in Figure 58 and one for ramp response depicted in Figure 59. The definition of t_{rr} for ramp recovery including all the related datasheet parameters like peak reverse recovery current I_{RM} and the reverse recovery charge Q_{rr} has already been thoroughly described in section 1.4.2. In summary the t_{rr} for ramp recovery is an important design parameter which must always be considered in switching applications, since the diode t_{rr} can limit the maximum switching speed.

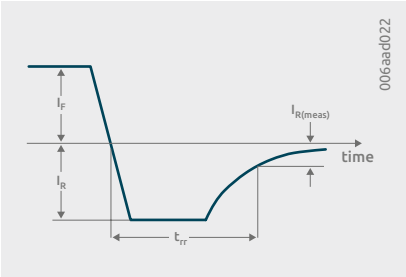


Figure 58 | Reverse recovery definition; step recovery.

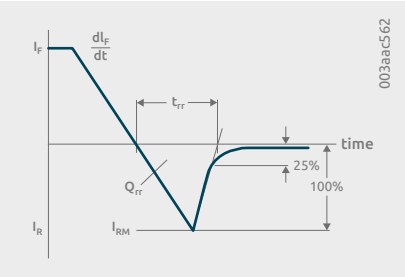


Figure 59 | Reverse recovery definition; ramp recovery.

The t_{rr} for a step recovery determines how long it takes the diode to restore blocking state after an instantaneous change of polarity. t_{rr} consists of two intervals in time. The first part is the delay caused due to removal of the stored charge in the form of excess carries into their respective region, which is called storage time. During this time, a negative current I_R is flowing through the diode. The time to recover from this to a specified reverse current level $I_{R(meas)}$ is called transition time. Diodes can be classified depending on their t_{rr} into fast and slow recovery diodes. t_{rr} can range from a few microseconds (PN junction) down to a few nanoseconds (Schottky diodes).

While the reverse recovery time describes the behavior when the diode changes from on to off state, the peak forward voltage is a measure of how much overshoot voltage drop will be present once the diode is turned on, before decreasing to V_F for the on state. Hence it is a measure for forward recovery tfr. Like t_{rr} for ramp recovery, the forward recovery is defined for a specified ramp as defined under conditions for this measurements in Table 20. The forward recovery definition is given in Figure 60.

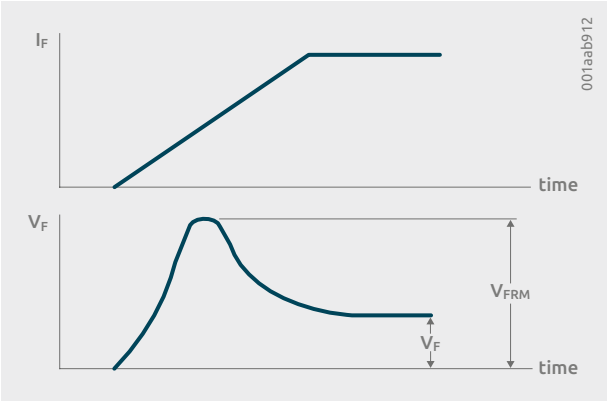


Figure 60 | Forward recovery definition.

Since such di/dt behavior is often present in switching application where a current limiting inductor is present, V_{FRM} is an important parameter to consider in the diode selection process diodes since it might impact conduction losses.

3.2.6 Datasheet temperature curves

The section covers the temperature curves which are part of the characteristics section.

Figure 61 shows the average reverse power dissipation $P_{R(AV)}$ as a function of V_R. In the off state there is power dissipation due to the leakage current through the diode being almost simultaneously present with a reverse voltage applied. The curves are given for a constant T_J of 100°C (self-heating is neglected in this graph) and different duty cycles δ. The duty cycle is the time where the diode is in reverse direction divided by the cycle time T. As expected for small δ, the average power dissipation is less compared to larger δ. Since the I_R increases exponentially as the V_R increases , $P_{R(AV)}$ increases as well with $P_{R(AV)} = V_R \times I_R$.

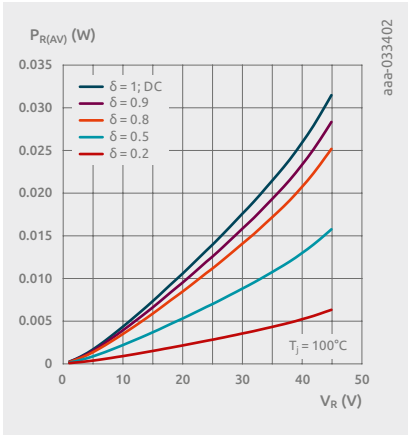


Figure 61 | Average reverse power dissipation as a function of reverse voltage; typical values.

The next two curves (Figure 62 and Figure 63) show the $I_{F(AV)}$ for a constant T_J of 175°C (maximum junction temperature) and different duty cycles as a function of T_{amb}. The switching frequency is set to 20kHz. The difference between the two curves is the mounting condition. Figure 62 shows $I_{F(AV)}$ for standard footprint and Figure 63 for a 1cm² mounting pad attached to the cathode. The curves are consistent to the Z_{th} graphs of the datasheet. The relation between I_{peak} and average forward current as a function of ambient temperature as well as the shape of the curves will be explained in the next chapter.

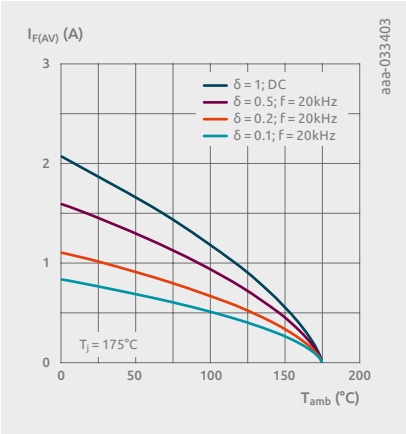


Figure 62 | Average forward current as a function of ambient temperature; typical values – standard footprint.

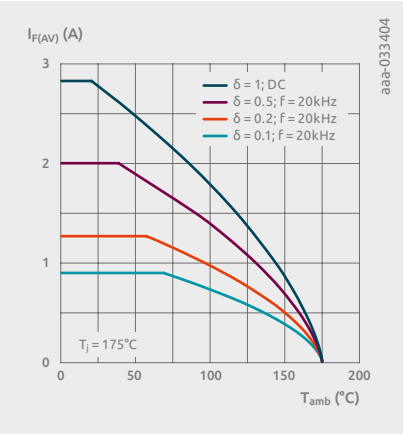
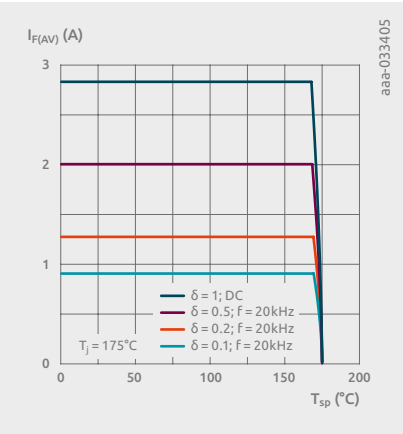


Figure 63 | Average forward current as a function of ambient temperature; typical values – 1cm² mounting pad.

Figure 64 | Average forward current as a function of solder point temperature; typical values.



In Figure 64, $I_{F(AV)}$ is depicted versus T_{sp}, so not versus T_{amb} as in prior diagrams. From Figure 64 the maximum allowable solder point temperature can be extracted from DC condition to pulsed operations.

The last set of curves describes derating V_{Rmax} with respect to the junction temperature for three different conditions. These graphs define basically the safe operating area of the diode in reverse direction:

1. Standard footprint on FR4 PCB ($R_{th(j-a)}$ = 230K/W) – Figure 65
2. Mounting pad for cathode 1cm² on FR4 PCB ($R_{th(j-a)}$ = 125K/W) – Figure 66
3. Soldering point of cathode tab $R_{th(j-s)}$ = 6K/W – Figure 67

These curves show that the derating of V_{Rmax} can be compensated to for a to certain amount degree by good thermal management on the PCB. For more details regarding safe operation are please refer to 4.3.

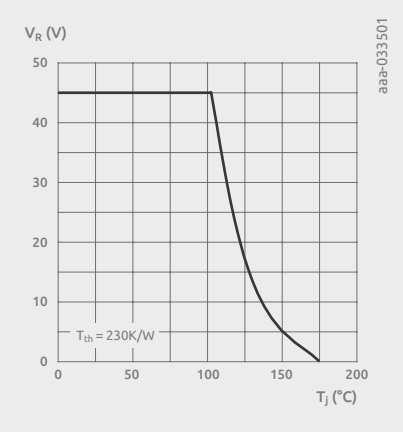


Figure 65 | Derated maximum reverse voltage as a function of junction temperature; typical values – thermal resistance junction to ambient as defined for standard footprint.

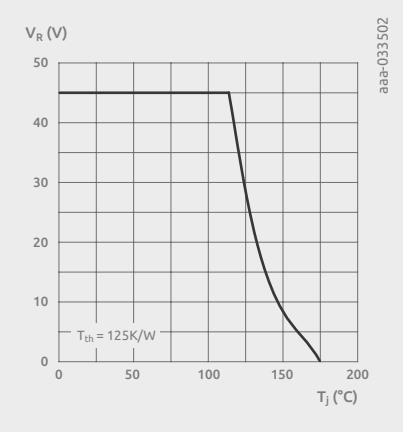


Figure 66 | Derated maximum reverse voltage as a function of junction temperature; typical values – thermal resistance junction to ambient as defined for 1cm² cathode mounting pad.

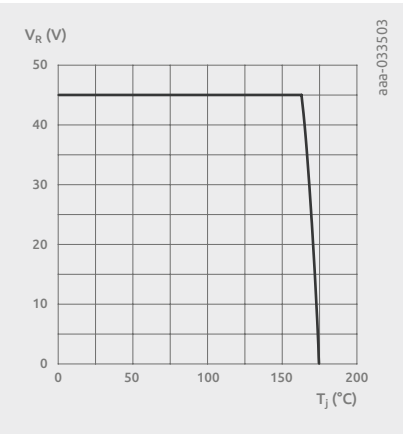


Figure 67 | Derated maximum reverse voltage as a function of junction temperature; typical values – thermal resistance of junction solder point $R_{th(j-s)}$ = 6K/W.

3.2.7 Package outline & recommended footprint for reflow soldering

The last two subsections provide information about the package outline in Figure 68, and the recommended footprint for reflow soldering shown in Figure 69.

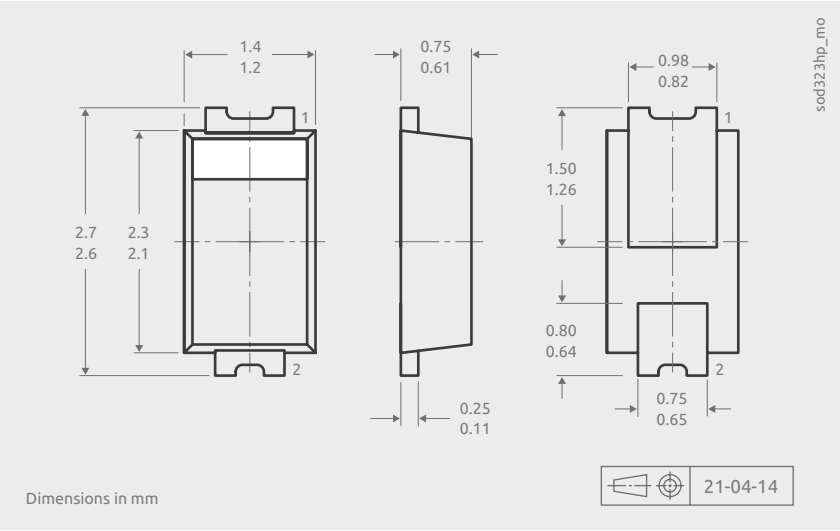


Figure 68 | Package outline CFP2-HP (SOD323HP).

The package outline is a technical drawing showing a first angle projection (European projection – indicated by the symbols in the bottom right corner Figure 68) of the package.

The recommend footprint for reflow soldering gives information about layer set up for the specific footprint with respect to solder resist (a protective layer against oxidation and which also prevents solder bridges from forming between closely spaced solder pads), solder paste (decides how bigdetermines the size of the opening for the solder pad is in the stencil) and solder land (the actual solder pad for the pin – often slightly bigger than the footprint itself). Additionally, the occupied area on the PCB can be derived from the drawing in Figure 69. All dimensions are provided in mm. The recommended stencil thickness for the CFP2-HP footprint is 0.1mm.

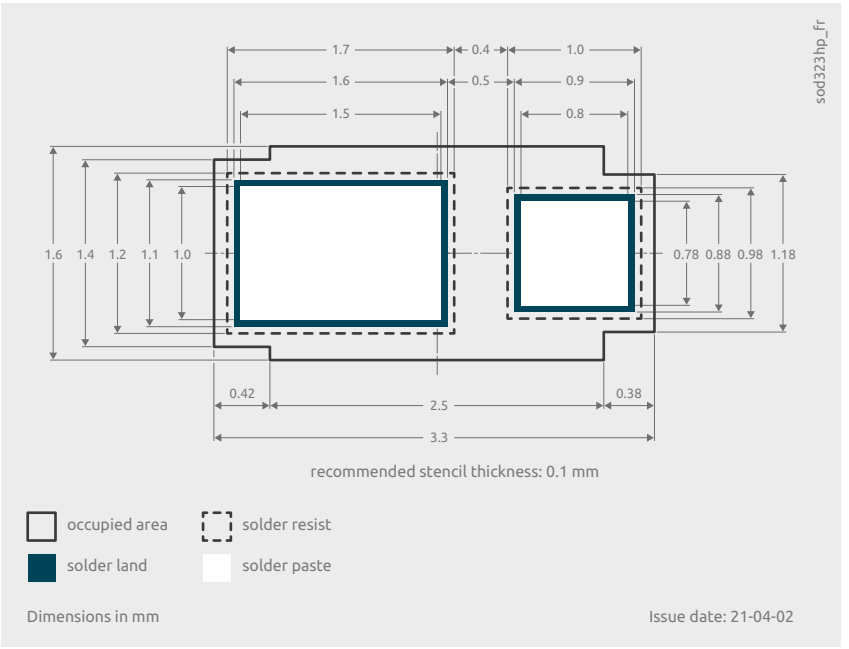


Figure 69: Reflow soldering footprint for CFP2-HP (SOD323HP).

Chapter 4

Thermal considerations

4.1 Diode as a thermal system

A typical small signal or medium power semiconductor device can be broken down to some major components which define the thermal behavior of the device.

Figure 70a shows a simple structure diagram of a wire bonded semiconductor device with its major component leadframe, semiconductor chip, wire bonding and encapsulation. For some of the more power-oriented package architectures, the wire bond is replaced with clip frame connection which is more comparable to the leadframe itself (further referred to as clip-bond packages). A diagram can be found in Figure 70b.

A third class of packages includes additional terminals with a comparably large area to allow the efficient dissipation of heat from the device to its surroundings, often referred to as 'package heatsink'. A diagram of a wire bonded device with a package heatsink is shown in Figure 70c. Also, the combination of a package heatsink with a clip frame is available for efficient heat dissipation and robust package performance (Figure 70d).

PCBs (printed circuit board) are the connection of small signal devices to the environments. They are suppling the electrical power to the device and they are also the main element to dissipate heat away from the device. For bigger power device packages (e.g. TO220) a second path can be present by adding a cooling element like passive heatsinks.

PCBs can have significant impact on the overall thermal device performance. They can limit the performance of the device or make use of the full potential of the device by smart design of the thermal dissipation paths. PCB design for good thermal behavior is a science of its own and will not be covered in detail in this handbook, except for a small excurse in section 3.1.4.

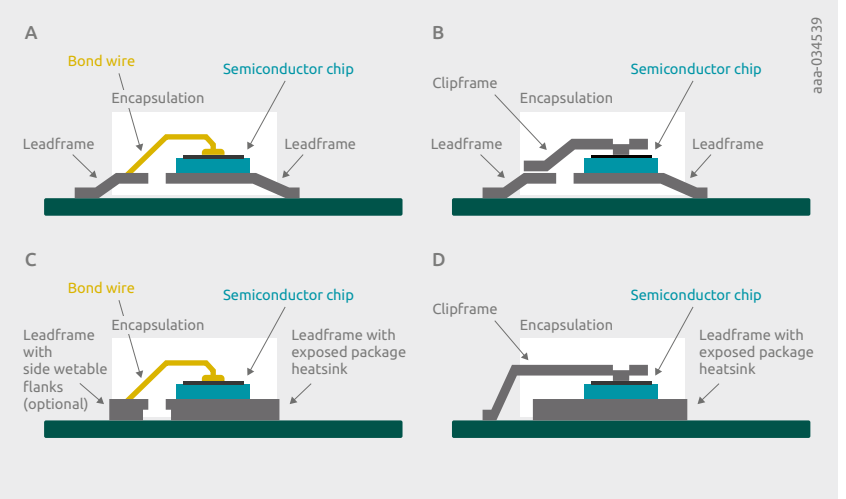


Figure 70 | A: wire bonded package, e.g. SOT23 – B: clip bonded package, e.g. CFP5.
C: wire bonded with package heatsink, e.g. DFN2020D-3.
D: clip bonded with package heatsink, e.g. LFPAK56 or CFP15B.

In the upcoming chapters the formal definition of thermal resistances as used by Nexperia will be given. This is followed by considerations of different package architectures and the discussion will conclude with some explanations that go beyond single chip semiconductor devices.

4.1.1 Measurement of thermal resistances

Team Nexperia measures the thermal resistances of its small signal devices on standardized PCBs with different footprints. The outcome is commonly shown in the datasheets of the devices as the $R_{th(j-a)}$ values for different PCBs.

The extraction of $R_{th(j-sp)}$ values follows the Transient Dual Interface Method (TDIM) according to JESD51-14 (alternative method on dedicated PCBs).

4.1.2 Definition of thermal resistances

A thermal resistance can be considered to be completely analogous to an electrical resistance. This analogy helps in many situations to help think 'thermally' when making decisions concerning heat dissipation.

Definition:
The resistance $R_{(X\text{-}Y)}$ is defined between two physical points as the temperature difference $\Delta T_{(X\text{-}Y)}$ between this points divided by the power $P_{(X\text{-}Y)}$ dissipated along the path between points X and Y:

$$R_{(X\text{-}Y)} = \frac{\Delta T_{(X\text{-}Y)}}{P_{(X\text{-}Y)}}$$

Reference points X and Y can be every point in the thermal system under investigation. In Nexperia datasheets, the common situation is point X to be the junction of the semiconductor device (T_j) and the point Y to be the solder point of the package or the ambient (temperature). This is depicted in Figure 71.

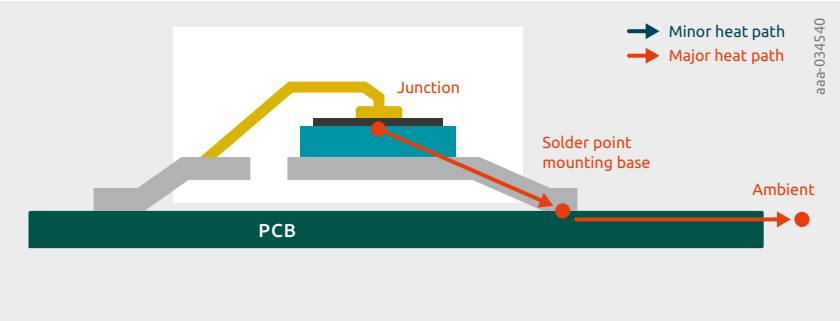


Figure 71 | Sketch showing the main heat flow.

In this way Nexperia defines and uses several common $R_{th(j\text{-}Y)}$ values as found in Table 21.

Table 21: Definition of common $R_{th(j\text{-}Y)}$ values.

Value	Sign	Description
Junction to ambient	$R_{th(j\text{-}a)}$	Overall thermal resistance of the system including package, solder joints, PCB and optional other thermal design relevant components.
Junction to solder point / mounting base	$R_{th(j\text{-}sp)}$ $R_{th(j\text{-}mb)}$	Thermal resistance of the device. Reference point on the outside of the package is the pin or package heatsink of the main heat dissipation path. *Mounting base* is mainly used for power oriented packages with a package heatsink, *solder point* is mainly used for smaller SMD or DFN packages.
Junction to top / case	$R_{th(j\text{-}top)}$ $R_{th(j\text{-}c)}$	Thermal resistance of the minor heat dissipation path from device junction to the hottest spot on the top surface of the device. This parameter is not used nor accessible in real applications without top side cooling (see 3.1.6 for details).
Solder point to ambient	$R_{th(sp\text{-}a)}$	Thermal resistance of the whole system without the packaged device. Reference point on the device side is always the connection point to the main heat dissipation path of the device. Ambient reference point is always the ambient air temperature (commonly 25°C or room temperature).
Coefficient junction to top	$Y_{(j\text{-}top)}$	Coefficient characterizing the temperature difference from device junction to the hottest spot on the top surface of the device in correlation to the overall device power. Strictly speaking not a thermal resistance (see 3.1.6 for details).

4.1.3 Approximations

Looking at the formal definition of a thermal resistance we can see that for the commonly used R_{th} values from Table 21 some approximations have been applied and there are inaccuracies which are commonly not spoken out in the field and datasheets.

Besides the main heat dissipation path shown in Figure 71 for a wire bonded semiconductor device, there are also minor heat dissipation paths, as shown in Figure 72.

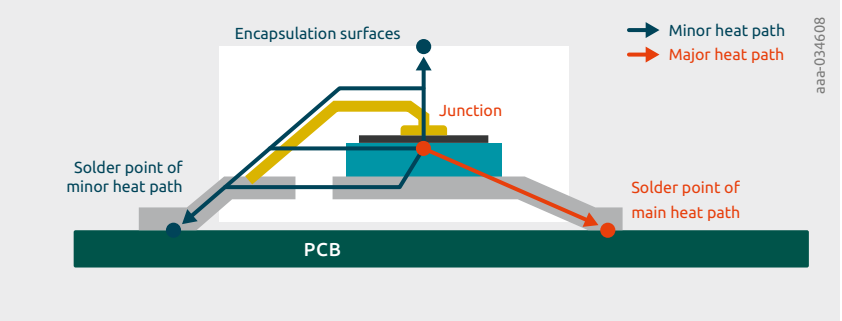


Figure 72 | Sketch highlighting minor heat dissipation paths.

Looking at $R_{th(j\text{-}a)}$ values, we can use the formula given in 3.1.2 to calculate the thermal resistance, since in the end, all power from the device is dissipated to the ambient between the reference points junction and ambient.

Looking at the $R_{th(j\text{-}sp)}$ values we come to the first approximation. The minor power dissipation paths as shown in Figure 72 are considered negligible and their contribution is omitted in the calculation of thermal resistances. In reality, the power dissipated between the reference points is lower than the overall power dissipated at the device.

For wire bonded devices this approximation is reasonable, since all the minor paths are low in contribution. The situation becomes more complex looking at clip bonded or multi die devices, or even at thermal resistances which are considered minor. The next chapters will cover clip bonded devices, multi die devices and will look at the commonly used '$R_{th(j\text{-}c)}$' or '$R_{th(j\text{-}top)}$' value.

4.1.4 Clip bonded packages

Clip bond packages differ thermally in one significant way from wire bonded packages. The heat dissipation from the junction of the device has two different paths it can follow, as shown in Figure 73. Along the leadframe, as for wire bonded packages and along the clipframe, which is a similarly good dissipation path as via the leadframe. This has some interesting implications and opportunities for thermal design of the PCB.

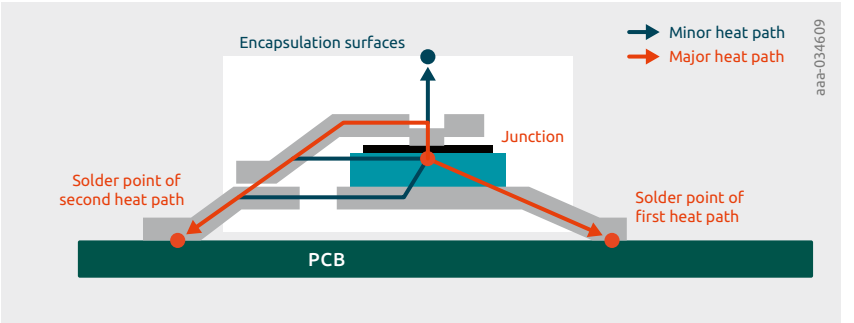


Figure 73 | Heat dissipation flow in clip-bonded packages.

Firstly, the definition of a $R_{th(j\text{-}sp)}$ value is not as straight forward as for wire bonded packages. While wire bonded packages have only one significant dissipation path, clip bonded packages have two. Looking at the definition of the thermal resistance this means that the solder reference point is split into two, which do not necessarily need to have the same temperature. The thermal resistance of the whole device is now a parallel network of two resistances, which do not necessarily need to be at the same reference point (temperature) on the side of the solder point.

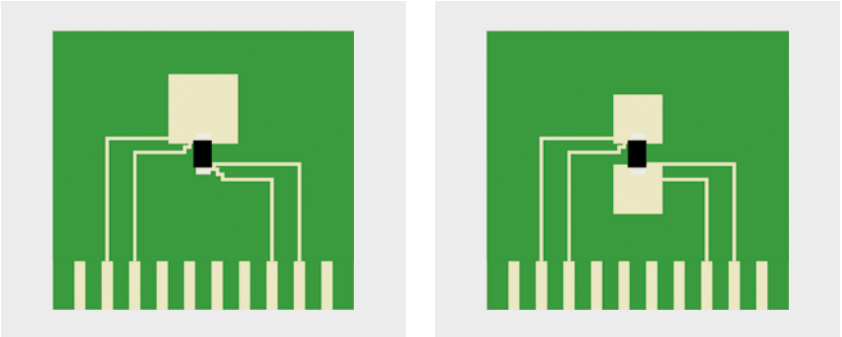
Nevertheless, Nexperia follows the same procedure to extract the $R_{th(j\text{-}sp)}$ values for clip bonded devices as for wire bonded devices. The value characterizes the main dissipation path through the die to the leadframe to the solder point (most of the time cathode pin). This makes the values of clip bonded products comparable to the wire bonded products, if used in a similar PCB layout. Nevertheless, the overall potential of the device is typically higher, since the second path is not used to its full possibilities while extracting the $R_{th(j\text{-}sp)}$ value.

The fact that there is a second significant dissipation path creates some good opportunities in PCB design. Whilst with wire bonded devices the only option is to remove heat via a single path (most via the cathode pin), with clip bonded devices both terminals can be used. This significantly improves the thermal performance of the system by offering good thermal paths on the PCB for all terminals. The following thermal simulation is intended to illustrate this.

The simulation of the heat dissipation in a PMEG6030ELP in CFP5 package shows that 35% of the heat can be transferred via the cupper clip into the anode pin while the heat dissipation through the leadframe into the cathode pin accounts for 65% of the overall heat dissipation. This means there is the potential to remove a significant amount of the dissipated power through the anode pin into the PCB.

This also gives the possibility to place the cooling pad for the diode on the PCB differently, if necessary for the PCB design. Simulations in Figure 74 show that with a 1cm² heatsink area at the anode pin instead at the cathode pin only a reduction of overall dissipated power of ~5% has to be accepted (assuming a maximum junction temperature of 150°C).

It is obvious that the additional heat dissipation path also offers the possibility to dissipate more power in the clip bonded package. By placing 0.5cm2 heat sink areas at each terminal of the package, as illustrated in Figure 74, it is possible to run the diode at the same junction temperature with approx. 20% more overall power dissipation compared to a standard design where only the cathode side has a heat sink the size of 1cm².



PCB type	Heatsink area at cathode pin (cm²)	Heat sink area at anode pin (cm²)	P_{tot} at T_j=150°C (mW)	
70µm Cu Single layer FR4 PCB	0.5	0.5	1337	106%
	1	0	1260	**100%**
	0	1	1190	94%
	6	0	1940	**100%**
	3	3	2329	120%

Figure 74 | Simulation results showing the potential of heat dissipation through the anode pin. By placing a 0.5cm² heat sink at each diode terminal on the PCB (top right picture) 20% more power can be dissipated at the same junction temperature of 150°C compared to the standard design with a 1cm² heat sink at the cathode pin only (top left picture).

4.1.5 Multiple chip devices

Devices with more than one chip can be very complex thermally in the real world, since the operational state of the first chip will influence the (thermal) behavior of the second and vice versa. Strictly speaking the $R_{th(j\text{-}sp)}$ of the first device is a function of the temperature of the second chip.

In datasheets, Nexperia gives the $R_{th(j\text{-}sp)}$ of one of the chips while the second one is inactive (no heat generation). This is the same approach as for the clip bonded devices, where the $R_{th(j\text{-}sp)}$ is retrieved in the same way as for all single chip wire bonded devices. In this way also the $R_{th(j\text{-}sp)}$ values of dual or multi chip devices are comparable to the single chip devices and each chip of the device can be characterized independently. Since the vast majority of multi-chip devices are symmetric dual chip devices, we only give one valid $R_{th(j\text{-}sp)}$ value for each chip in the device (while the others are inactive).

To give a rough overview on what the influence of the second chip in the device is, thermal resistances $R_{th(j\text{-}a)}$ are given 'per chip' (only one chip active) and 'per device' (both chips on the same T_j). These are the corner stones of the thermal range the whole device can be operated in.

4.1.6 $R_{th(j\text{-}c)}$ and why Nexperia calls it Ψ(j-top)

The topic of $R_{th(j\text{-}c)}$ can be confusing. There are several definitions of this resistance and most of the time it is not stated clearly what is meant by this parameter. From discussions with customers we see that some people consider it to be the thermal resistance of the device from junction to a package heatsink (e.g. screw hole of TO220), which would be the same as Nexperia's $R_{th(j\text{-}sp)}$ or $R_{th(j\text{-}mb)}$ values. Others refer to it as the thermal resistance from the junction of the device to the top of the plastic body of the package. This is a thermal resistance on a minor heat dissipation path and some implications need to be considered when working with this parameter.

Most of the time, the $R_{th(j\text{-}c)}$ parameter for small signal devices can be thought of as the relation of the top package temperature to the junction temperature in relation to the power dissipated over the device. The application behind this is the measurement of the top package temperature with an IR camara to calculate the junction temperature together with the overall power dissipated in the device. This is perfectly valid, but some considerations need to be taken into account. These considerations are the reason why Nexperia calls this parameter $Y_{(j\text{-}top)}$.

Firstly, we need to know that we are looking at a minor heat dissipation path, which is usually neglected in the overall picture (compare Figure 72). If we follow strictly the definition of a thermal resistance (see 3.1.2) to calculate thermal resistance from junction to case (top of the package) $R_{th(j-c)} = R_{th(j-top)}$ we need to take the temperature difference from the junction of the device to the top of the package and divide it by the power dissipated along the same (!) path. Note: this is not the overall power of the device in operation, nor is it close to it. It is a fraction of the overall power which is for most small signal devices below 1% of the overall power consumption. Or to put it in other words, the real $R_{th(j-top)}$ is not accessible in real applications nor is it useful for the purposes of calculating the junction temperature via the top package temperature and the overall device power consumption.

The coefficient in question is, strictly speaking, not even a thermal resistance, since temperature difference and power dissipation path differ from each other. Therefore, Nexperia calls this coefficient $Y_{(j-top)}$.

As in the previous chapters concerning clip bonded packages or multiple die devices, we are considering heat as a resistor network. Again, the parameter is now dependent on the condition of the reference points. We need to take into account that the proportions of the heat going through the different dissipation paths (major and minor) may shift depending on the ambient conditions. For example, devices on a PCB with an overall low $R_{th(sp-a)}$ dissipate a higher percentage of the power over the main dissipation path than devices on a PCB with high thermal resistance. In consequence, the relations between these two paths is shifted and the value of $Y_{(j-top)}$ changes with the ambient conditions.

It is not only the PCB that will affect this value. All ambient conditions which affect the heat dissipation from the device will do so: e.g. forced air flow or free air flow; high overall temperature level or low overall temperature level; temperature gradients or even heat radiation from nearby surfaces. The $Y_{(j-top)}$ parameter is currently only available on request and there will be no single value, always a range. The parameter is retrieved via thermal simulations of the system on different PCB layouts (i.e. ambient conditions).

4.2 Thermal considerations in forward bias

As with any other electronic device, diodes have to be operated within the maximum junction temperature as defined in the data sheet. In forward bias, power is dissipated in the device, increasing the junction temperature. The resulting temperature rise must not exceed the specified maximum junction temperature. If the specified junction temperature is exceeded the reliability of the diode may be affected leading to failures.

4.2.1 Continuous current

In case of a continuous forward current, the rated current through the diode can be easily calculated. The following input is needed to calculate this: the specified maximum junction temperature T_{jmax}; the specified thermal resistance junction to ambient according to the utilized PCB type and the footprint; the ambient temperature T_a ; and the forward voltage drop V_F at rated T_{Jmax} and at the appropriate value of I_F:

$$I_F = \frac{T_{jmax} - T_a}{V_F \times R_{th(j-a)}}$$

This equation can be solved for T_a to calculate the maximum ambient temperature for a given forward current.

4.2.2 Pulsed operation

In a pulsed operation the junction temperature also depends on the width and the duty cycle of the pulse. As these are dynamic processes, it is now necessary to use the thermal impedance Z_{th} rather than the steady-state thermal resistance R_{th}. The thermal impedance is specified in the data sheet of the diode based on the thermal response curve, as described in 0. With a current pulse of a given pulse width t_p, duty cycle δ and peak current I_{peak} the maximum tolerable ambient temperature is can be calculated from:

$$T_a = T_{jmax} - I_{peak} \times V_F \times Z_{th(j-a)}(\delta, t_p)$$

T_{jmax} is here again the maximum specified junction temperature. V_F is the forward voltage drop at rated T_{Jmax} and $Z_{th(j-a)}(\delta, tp)$ is the thermal impedance junction to ambient being a function of the pulse width t_p and the duty cycle δ.

This equation can also be used to calculate the peak current, the average current and the root mean square of the current for a given ambient temperature. The following example is a rectangular signal:

$$I_{peak} = \frac{I_{average}}{\delta} = \frac{I_{rms}}{\sqrt{\delta}} = \frac{T_{jmax} - T_a}{V_F \times Z_{th(j\text{-}a)}(\delta, t_p)}$$

This is also how the graphs in the data sheets are calculated, and with which manufacturers indicate the average current depending on the ambient temperature and the solder point temperature for a given switching frequency, as shown in Figure 75. If the solder point temperature is selected as the reference point, the equations shown above still apply, only the ambient temperature is replaced by the solder point temperature.

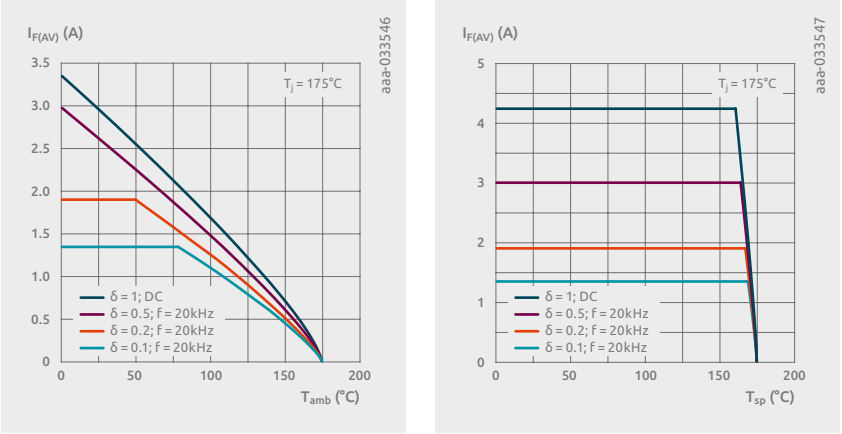


Figure 75 | Average forward current of an exemplary diode as a function of the duty cycle and of the ambient temperature of solder point temperature.

Please notice that the average currents in Figure 75 are bordered by plateaus. The plateaus are set by the manufacturers, defining a maximum root mean square current through the diode. This value is defined by the current carrying capability of the connections inside the package and the external connections.

4.3 Thermal considerations in reverse bias

In the reverse direction, the device self-heating caused by the leakage current of the diode is extremely important for a safe operation of the diode. The boundaries for safe operation of the diode in reverse bias are defined by the safe operating area (SOA) graph of the diode in its data sheet. Operating a rectifier within its safe operating area with a sufficient safety margin is crucial for a robust design, especially at the high ambient temperatures seen in high power density or high temperature automotive applications. This section describes what thermal stability and the associated thermal runaway of the diode mean; subsequently, the calculation of the SOA is demonstrated. The main factors influencing the thermal limits of a rectifier are discussed.

4.3.1 Rectifier as thermal system – thermal runaway

The thermal stability of a rectifier in reverse direction is determined by the interaction of its leakage current which causes self-heating, and the capability of the rectifier to dissipate this heat through the thermal resistance in the system. In thermal equilibrium, the junction temperature of the device can be described as follows with a fixed ambient temperature Ta as thermal 'ground':

$$T_j = R_{th(j\text{-}a)} \times P_{dissipated} + T_a$$

where $R_{th(j\text{-}a)}$ is the thermal resistance between junction and ambient, and $P_{dissipated}$ is the amount of dissipated power in the device.

A steady state condition is achieved as the result of two competing processes: the capability of the thermal system to dissipate heat through the thermal resistance (as described by the formula above) and the self-heating of the device ($P_{generated}$) generated by its own reverse leakage current (and, technically-speaking, also by possible switching losses), with increasing leakage current over the junction temperature. These processes are shown in Figure 76.

In Figure 76, the curve representing the dissipated power intersects the x-axis at ambient temperature and then rises with a slope which is proportional to the thermal conductance ($1/R_{th}$) of the system. The generated power caused by the leakage current of the diode increases exponentially when the junction temperature increases, as the leakage current increases exponentially over temperature. The intersections of the two curves give the co-ordinates for an equilibrium condition. The first intersection corresponds to the stable operation of the system. As long as the generated power through self-heating is smaller than

the dissipated power, the junction temperature of the device decreases and, in thermal equilibrium, converges toward a stable condition. Interestingly, this simple model also explains the heating-up of the device when the system is switched on, as the junction temperature converges to the stable condition (illustrated in Figure 76 by the red arrow pointing to the stable condition).

However, if more power is generated than dissipated (intersection representing unstable operation) the junction temperature increases until the device eventually becomes thermally unstable. This is termed 'thermal runaway'. The device will draw more and more current until it fails completely due to thermal overstress. Figure 77 shows an x-ray picture of a device which has failed due to thermal runaway. In this case, the fusing current of the wire bond has been exceeded. In the case of clip bond packages, the die itself would be destroyed by thermal overstress. The discoloration of the epoxy molding compound testifies to the high heat experienced by the device.

The temperature gap between stable and unstable operation is the safety margin of the system. With an increase in ambient temperature, this safety margin shrinks until the stable and the unstable conditions coincide (Figure 78). This is obviously the case when the condition $\frac{dP_{generated}}{dT} = \frac{1}{R_{th}}$ occurs.

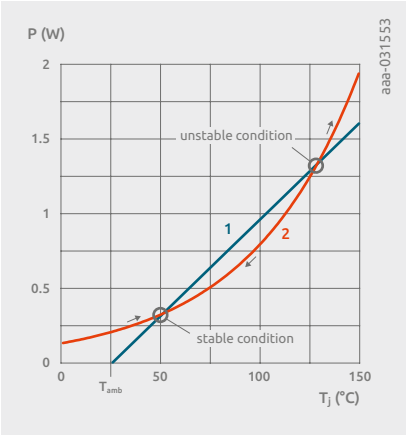


Figure 76 | The equilibrium condition is the outcome of two parallel processes: the generated power (self-heating) caused by the reverse leakage current of the rectifier (red line – nr. 2) and the capability of the system to dissipate power through the thermal conductance (blue line – nr. 1). The intersections of the two graphs are the co-ordinates where this occurs. The values of x and y axes are exemplary.

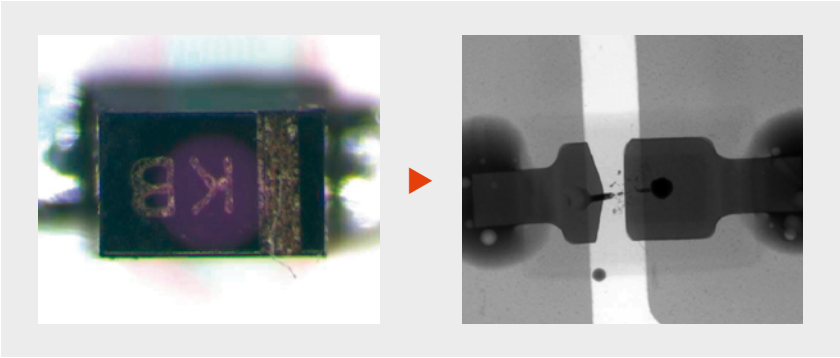


Figure 77 | Failed device due to thermal runaway. The X-ray picture reveals that the fusing current of the wire bond has been exceeded. In the left hand picture, the epoxy molding compound is discolored through the heat.

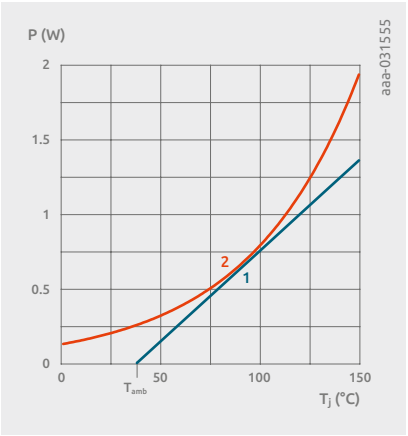


Figure 78 | With an increase in ambient temperature, the dissipated power curve (line 2) moves along the x-axis while the generated power curve (line 1) remains unchanged. The safety margin shrinks until the stable and the unstable conditions coincide and the condition $\frac{dP_{generated}}{dT} = \frac{1}{R_{th}}$ for thermal runaway is fulfilled.

4.3.2 The safe operating area (SOA) of a rectifier in reverse direction

The limits given by the thermal runaway condition define the safe operating area of a rectifier in reverse direction. For each reverse bias voltage, V_R, the corresponding leakage current, I_R, is measured over junction temperature. By applying the formula:

$$\frac{dP_{generated}}{dT} \times R_{th} \geq 1 \; (with \; P_{generated} = V_R \times I_R)$$

the temperature limit for thermal runaway can be calculated for each reverse bias point for a given R_{th}. As a result, a curve is generated which shows the maximum thermally stable reverse voltage for a rectifier based on its junction temperature, as shown in Figure 79. In practice, the SOA graph in Figure 79 is used as follows:

for a given application where the $R_{th(j\text{-}a)}$ of the product is known, the requested maximum reverse voltage defines the maximum junction temperature according to this graph. Now, the generated power can be calculated by taking into account the leakage current of the device at the given reverse voltage and junction temperature as given in the rectifier datasheet. Finally the maximum allowable ambient temperature can be easily calculated:

$$T_{amb\_max} = T_{j\_max} - P_{generated} \times R_{th(j\text{-}a)}$$

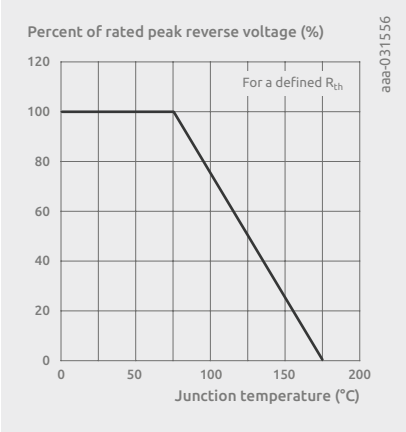


Figure 79 | Plotting the maximum reverse voltage and junction temperature of the rectifier. For a given R_{th}, the derating curve defines the maximum reverse voltage the rectifier can withstand before going into thermal runaway.

4.3.3 Impact of technology on the SOA of a rectifier

According to the formula $\frac{dP_{generated}}{dT} = \frac{1}{R_{th}}$ there is a strong impact of the thermal resistance of the system on the SOA of the rectifier as described in previous section. As a result, the SOA of a rectifier can be extended by using packages with a low junction-to-solder-point thermal resistance $R_{th(j\text{-}sp)}$, and/or by using PCBs or substrates with improved thermal properties, e.g. ceramic PCBs.

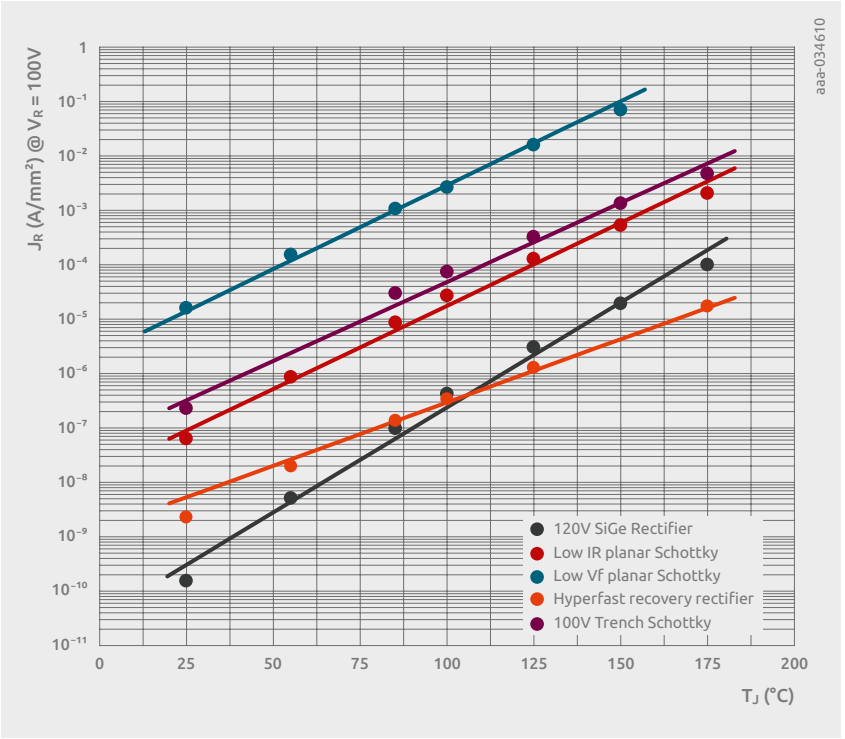


Figure 80 | Leakage current density of five different rectifier technologies measured at 100V reverse bias over temperature.

Another important aspect is the impact of the chosen rectifier technology on the SOA, as the generated power is caused by the reverse leakage current of the rectifier at a given bias point. In order to compare the leakage current of different technologies, it makes sense to use the leakage current density rather the leakage current itself. This method eliminates the impact of the die size and makes a fair comparison of the different technologies possible. The graphs in Figure 80 show the behavior of the leakage current density at the reverse voltage of 100V depending on the junction temperature for five different technologies. The chosen technologies are as follows:

- 100V low leakage current planar Schottky;
- 100V low V_F planar Schottky;
- 200V hyperfast recovery rectifier;
- 120V SiGe (silicon germanium) rectifier
- 100V Trench Schottky

As expected, the highest leakage current density is observed for the low V_F Schottky rectifier technology, since this uses a Schottky metal with a low work function. The leakage current density of the low leakage planar Schottky technology is two orders of magnitude lower, showing the exponential impact of the barrier height on the leakage current. A very low reverse current density is achieved by the hyperfast recovery rectifier (an even lower leakage current can be expected for recovery rectifiers with standard switching speeds, not shown in this comparison). Interestingly, the leakage current density for the novel SiGe rectifier technology is at the same level as for the hyperfast recovery rectifier. The Trench Schottky technology reveals a slighter higher reverse leakage current density over temperature compared to the low leakage planar Schottky. This illustrates the improved IR/V_F trade-off of the Trench technology, as described in section 1.2.3.

The decisive factor in determining the thermal stability of the rectifier in reverse direction is not the leakage current itself but the increase rate in leakage current over temperature. Therefore, the graphs in Figure 80 need to be differentiated with respect to temperature. The results are shown in Figure 81. Due to the exponential progress of the reverse leakage current density over the temperature, its derivative is also exponential and therefore linear on a log-scale. After the derivation (as indicator of thermal stability according to $\frac{dP_{generated}}{dT} = \frac{dI_R}{dT} \times V_R > \frac{1}{R_{th}}$) the order remains the same, with SiGe and hyperfast technologies showing the highest potential for thermal stability and the low V_F planar Schottky with the lowest potential in this regard.

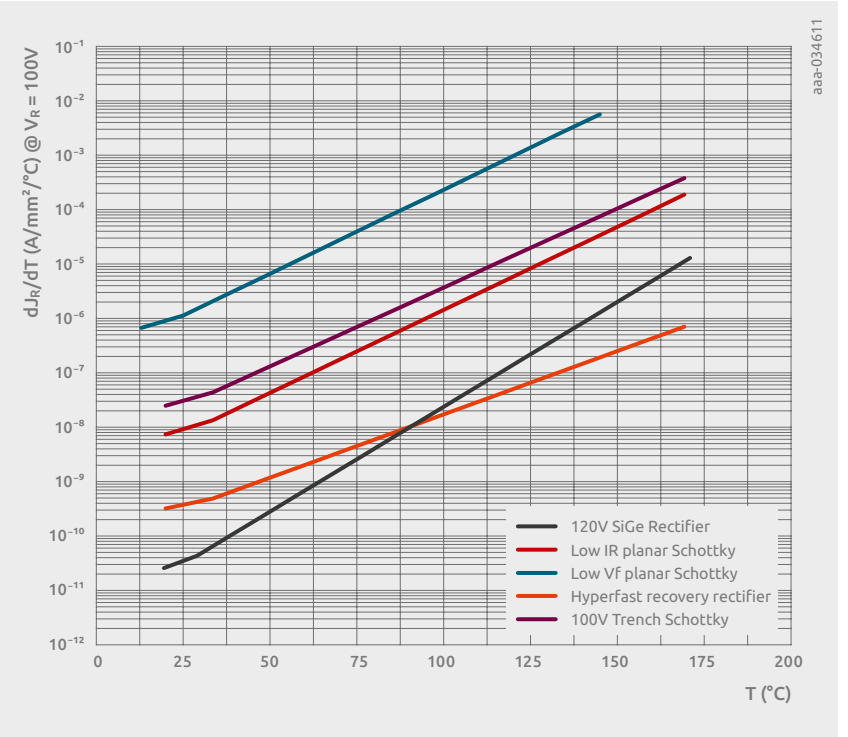


Figure 81 | Derivative of leakage current density at 100V reverse bias with respect to junction temperature for different rectifier technologies.

4.3.4 Impact of package on the SOA of a rectifier

In order to study the influence of the package on the safe operating area for a given technology, it is again necessary to use normalized currents to exclude the influence of crystal sizes. As a consequence, the thermal resistance must also be normalized. For this purpose, the thermal resistance is normalized with respect to the package size (strictly speaking, to the footprint area). In this way a stability factor can now be calculated for a given reverse voltage:

$$\frac{dJ_R}{dT} \times V_R \times R_T$$

With R_T being the normalized thermal resistance of the system.

As long as this equation remains below 1 the system is thermally stable; systems with values greater than 1 will eventually get thermally unstable. Following up on Figure 81, the stability limits are shown for different technologies in SOT23. For this comparison, the $R_{th(j-a)}$ of a SOT23 on standard footprint and single layer PCB has been normalized with respect to recommended footprint area of SOT23. This result states that under these conditions, a planar low V_F Schottky diode in 100V reverse bias can only be operated up to a junction temperature of 41°C without thermal runaway. The SiGe diode and the hyperfast recovery rectifier on the other hand can handle junction temperatures beyond 150°C without becoming thermally unstable. Now for comparison let's do the same exercise for the DFN package DFN1110D-3 (SOT8015). As described in 4.3.1 below, DFN packages are very compact housings that are nevertheless thermally excellent. The results are shown in Figure 83. The stability limit for the planar low V_F Schottky technology at 100V reverse voltage is shifted to $T_j = 62°C$. This results highlights the high thermal potential of DFN packages despite the much smaller package size. Keep in mind that the absolute value of thermal resistance junction to ambient for this package is bigger than for SOT23. However, this value is achieved on a much smaller footprint.

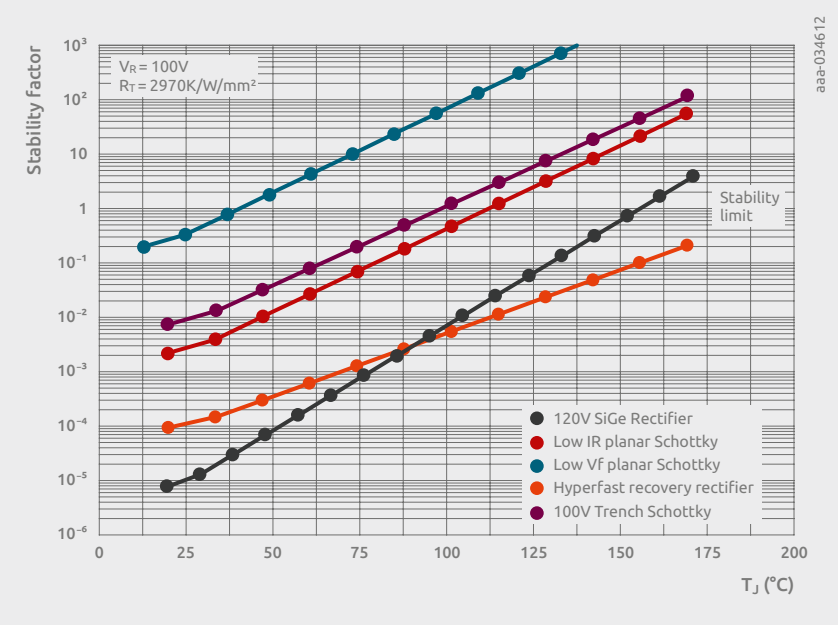


Figure 82 | Stability factors for different technologies in SOT23 package at 100V reverse voltage. For stability factors greater than 1 (stability limit), the rectifier will become thermally unstable. For this comparison the $R_{th(j-a)}$ of SOT23 on a standard footprint on a single layer PCB has been normalized with respect to recommended footprint area of SOT23.

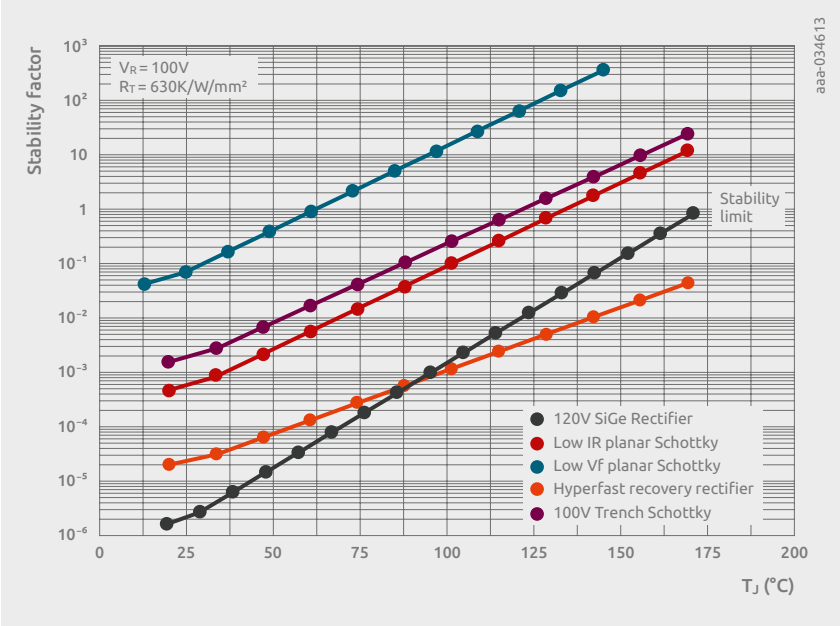


Figure 83 | Stability factors for different technologies in DFN1110D-3 (SOT8015) package at 100V reverse voltage. For stability factors greater than 1 (stability limit), the rectifier will become thermally unstable. For this comparison the $R_{th(j-a)}$ of DFN1110D-3 on a standard footprint on a single layer PCB has been normalized with respect to recommended footprint area of this package.

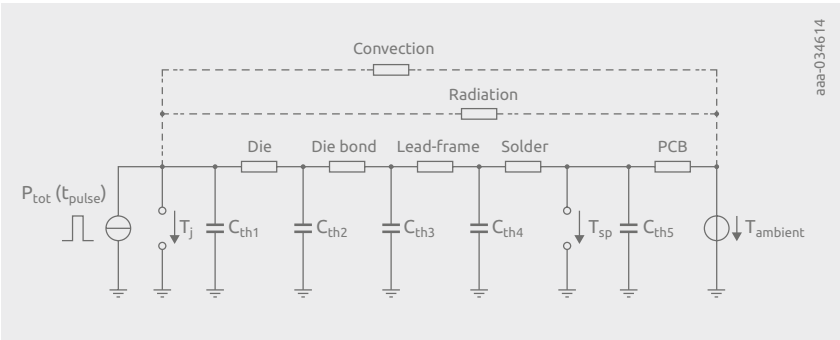


Figure 84 | A diode in a SMD package as thermal system. The heat is transferred from the reference point "j" (junction) to the reference point "ambient". For transient processes not only the thermal resistances need to be considered but also the thermal capacitances in the system, which, according to the electrical analogy, must first be charged before the heat can spread. The dynamic thermal impedance describes this heat transfer: $Z_{th(j-a)}(t_{pulse}) = \frac{\partial T}{\partial P_{tot}}$.

4.4 Transient effects

In pulsed applications, the device as the thermal system might not reach the steady state condition during the course of operation. In this case it does not make sense to use the steady state thermal resistance, rather the dynamic thermal impedance must now be used.

4.4.1 The dynamic thermal impedance Z_{th}

The dynamic thermal impedance Z_{th} basically describes the time dependence of the heat transfer. For transient processes not only the thermal resistances need to be considered but also the thermal capacitances in the system, which, according to the electrical analogy, must first be charged before the heat can spread (Figure 84). This transient heat flow between two reference points, A and B, resulting in a temperature difference between these points, is described by the dynamic thermal impedance Z_{th} which is a function of the applied pulse to the system:

$$Z_{th(A-B)}(t_{pulse}) = \frac{\partial T}{\partial P} \mid t = t_{pulse}$$

As described in chapter 2, the Z_{th} values are specified as a set of curves in the data sheet. They can be used to calculate the heating of the diode as a thermal system under pulsed conditions. Here, the pulse width and the duty cycle of the signal must be taken into account.

4.4.2 Foster and Cauer model

As shown in Figure 84 the dynamic thermal behavior of discrete semiconductor devices can be described by a RC thermal network. Foster and Cauer models are equivalent electrical representations of the thermal RC network that can represent the thermal performance of a discrete device, and used within a SPICE environment. This section provides some basic theory behind the principle, and how to implement Foster and Cauer RC thermal models. For convenience, Foster and Cauer RC thermal models are referred to as RC models in the following pages. Several methods of using RC thermal models, including worked examples, will be described.

RC models are derived from the heat-up curves based on the dynamic thermal impedance of a device, as shown in Figure 85 for PMEG050T150EIPD. As already described in chapter 3, this Figure represents the thermal behavior of a device under transient power pulses. Z_{th} can be generated by measuring the power losses as a result of applying a step function of varying time periods.

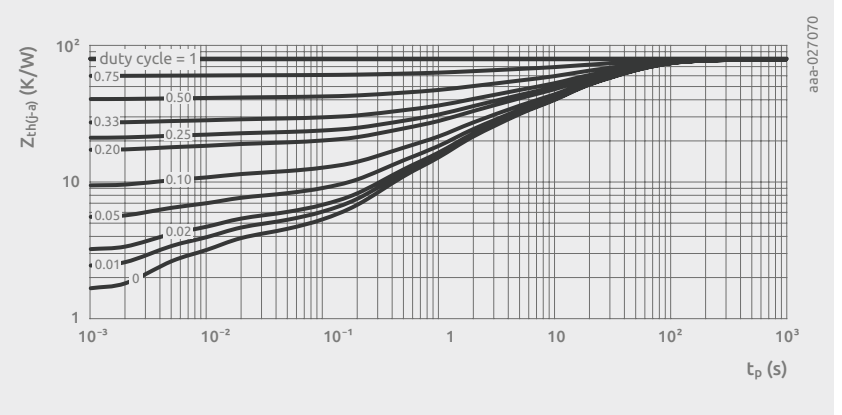


Figure 85 | Transient thermal impedance for PMEG050T150EIPD from junction to ambient as a function of pulse duration and duty cycle. Device mounted on standard footprint and on a single layer FR4 PCB; typical values.

According to Figure 85, a device subjected to a power pulse of duration >200 seconds, i.e. steady-state, has reached thermal equilibrium and the Z_{th} plateaus becomes the R_{th}. The Z_{th} illustrates the fact that materials have thermal inertia. Thermal inertia means that temperature does not change instantaneously. As a result, the device can handle greater power for shorter duration pulses. Z_{th} curves for repetitive pulses with different duty cycles are also shown in Figure 85. These curves represent the additional RMS temperature rise due to the dissipation of RMS power.

Calculating junction temperature rise

To calculate the temperature rise within the junction of a semiconductor device with a single active area (i.e. heat source at the junction), the power and duration of the pulse delivered to the device must be known. If the power pulse is a square, then the dynamic thermal impedance can be read from the Z_{th} chart. The product of this value with the power gives the temperature rise within the junction. If constant power is applied to the device, the steady state thermal impedance can be used i.e. R_{th}. Again the temperature rise is the product of the power and the R_{th}.

For a transient pulse e.g. sinusoidal or pulsed, the temperature rise within the device junction becomes more difficult to calculate.

The mathematically-correct way to calculate T_j rise after an event with the duration τ is to apply the convolution integral. The calculation expresses both the power pulse and the Z_{th} curve as functions of time, and use the convolution integral to produce a temperature profile:

$$\Delta T_j = \int_0^{\tau} P(t) \frac{dZ_{th}(\tau - t)}{dt} dt$$

However, this is difficult as the $Z_{th}(\tau - t)$ is not defined mathematically. An alternative way is to approximate the waveforms into a series of rectangular pulse and apply superposition. While relatively simple, applying superposition has its disadvantages. The more complex the waveform, the more superpositions that must be imposed to model the waveform accurately.

To represent Z_{th} as a function of time, we can draw upon the thermal electrical analogy and represent it as a series of RC charging equations or as an RC ladder. Z_{th} can then be represented in a SPICE environment for ease of calculation of the junction temperature.

Association between thermal and electrical parameters

The thermal electrical analogy is summarized in Table 22. If the thermal resistance and capacitance of a semiconductor device is known, electrical resistances and capacitances can represent them respectively. Using current as power, and voltage as the temperature difference, any thermal network can be handled as an electrical network.

Table 22: Elements of electrical and thermal analogy.

Type	Resistance	Potential	Energy	Capacitance
Electrical (R = V/I)	R = ohmic resistance (Ohms)	V = electrical potential (Volts)	I = current (Amps)	C = capacitance (Farads)
Thermal (R_{th} = K/W)	R_{th} = thermal resistance (K/W)	K = temperature difference (Kelvin)	W = dissipated power (Watts)	Cth = thermal capacitance (thermal mass)

Foster and Cauer RC thermal models

Foster models are derived by semi-empirically fitting a curve to the Z_{th}, the result of which is a one-dimensional RC network shown in Figure 86 . The R and C values in a Foster model do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants as can be in other modeling techniques. Finally, a Foster RC model cannot be divided or connected through, i.e. have the RC network of a heat sink connected.

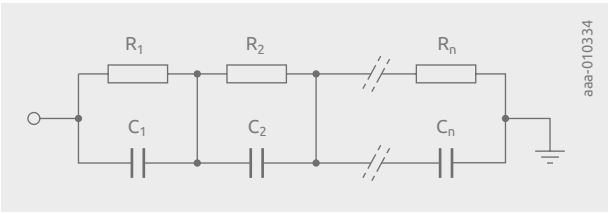


Figure 86
Foster RC thermal model.

Foster RC models have the benefit of ease of expression of the thermal impedance Z_{th}. For example, by measuring the heating or cooling curve and generating a Z_{th} curve, the following equation can be applied to generate a fitted curve as shown in Figure 87:

$$Z_{th}(t) = \sum_{i=1}^{n} Ri \times (1 - e^{-\frac{t}{\tau_i}}) \text{ where } \tau_i = R_i \times C_i$$

The model parameters Ri and Ci are the thermal resistances and capacitances used to create the thermal model depicted in Figure 86. The parameters in the analytical expression can be optimized until the time response matches the transient system response by applying a least square fit algorithm.

The individual expression, 'i', also draws parallels with the electrical capacitor charging equation. Figure 87 shows how the individual Ri and Ci combinations sum up to make the Z_{th} curve.

Foster models have no physical meaning since the node-to-node heat capacitances have no physical reality. However, a Foster model can be converted into its Cauer counterpart by means of a mathematical transformation.

An n-stage Cauer model can be derived from an n-stage Foster model and they will be equivalent representations of the device thermal performance.

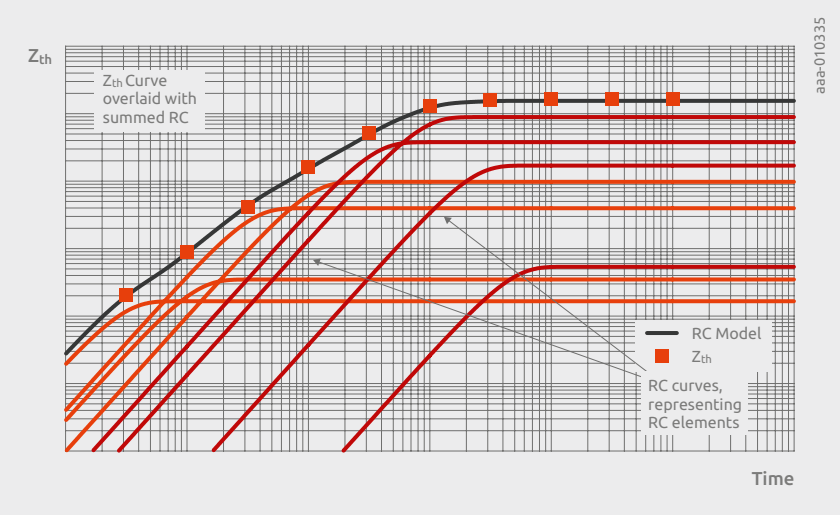


Figure 87 | Foster RC thermal model. Individual Ri and Ci combinations sum up to make the Z_{th} curve.

As seen for the Foster model, the Cauer model also consists of an RC network but the thermal capacitances are all connected to the thermal ground, i.e. ambient temperature as represented in Figure 88. The nodes in the Cauer model can have physical meaning and allow access to the temperature of the internal layers of the semiconductor structure.

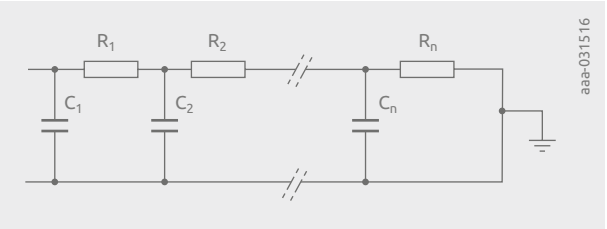


Figure 88
Cauer RC thermal model.

Nexperia provides Foster and Cauer RC models for many of its products on the product information pages. The models can be found under the tabs 'Documentation' and 'Support'. Foster and Cauer RC thermal models allow application engineers to perform fast calculations of the transient response of a package to complex power profiles. In the following sections, examples of using RC thermal models will be presented. Foster models and Cauer models are equivalent representations of the device thermal behavior but in the described examples Cauer models will be used as more representative of the physical structure of the device.

Table 23: PMEG050T150EIPD Cauer model netlist

**********			
* Part: PMEG050T150EIPD			
* Cauer style thermal RC network model of $R_{th(j-sp)}$.			
**********			
.subckt cauer 1 6 7			
R1	1	2	0.113734
R2	2	3	0.0998565
R3	3	4	0.229452
R4	4	5	0.346807
R5	5	6	0.0136469
C1	1	7	0.00317279
C2	2	7	0.00101058
C3	3	7	0.00491032
C4	4	7	0.00614301
C5	5	7	0.0274844
.end cauer			

The netlist in Table 23 describes the Cauer network and can be used to build the Spice schematic shown in Figure 89. Pin 1 in the netlist can be identified as the junction temperature pin T_j in the schematic. Similarly pins 6 and 7 as the Tamb pins in the schematic.

In order to simulate, only device pins 6 and 7 are tied to the ambient voltage source, as shown in Figure 89. One of the advantages of using Cauer models is that external networks can be added to the device model, for example to model PCBs and heatsinking. In order to do so, pin 7 will be tied to ambient, and pin 6 to the first pin of the external Cauer network. For correct results, the end pin of the external Cauer network must be tied to the ambient source.

Thermal simulation example

RC thermal models are generated from the Z_{th} heat-up curves. This example shows how to work back from the RC model and plot a Z_{th} curve within a SPICE simulator. This makes it easier when trying to read values of the Z_{th} curve from the data sheet.

This example and subsequent others use the RC thermal model of PMEG050T150EIPD. Tsp represents the solder point temperature. It is treated as an isothermal, and for this example is set at 0°C. A single shot pulse of 1 W power is dissipated in the device. For a single shot pulse, the time period between pulses is infinite and therefore the duty cycle δ = 0. Thus the junction temperature T_j represents the transient thermal impedance Z_{th}.

$$T_j = T_{sp} + \Delta T = 0°C + \Delta T = \Delta T$$
$$\Delta T = P \cdot Z_{th} = 1W \cdot Z_{th}$$

The equation above demonstrates that with P = 1W, the magnitude of Z_{th} equates to ΔT. The following steps are used to set up and run simulations:

1. Set up the RC thermal model of PMEG050T150EIPD in SPICE as shown in Figure 89
2. Set the value of voltage source Vsolderpoint to 0, which is the value of Tsp
3. Set the value of the current source Ptot to 1
4. Create a simulation profile and set the run time to 100 ms
5. Run the simulation
6. Plot the voltage at node T_j

The simulation result in Figure 90 shows the junction temperature (voltage at T_j) which is also the thermal impedance of PMEG050T150EIPD. The values of Z_{th} at different times can be read using the cursors on this plot within SPICE. The value of the current source in this example is set to 1 A to represent 1 W dissipating through the device. It can be easily changed to represent any value of power. The simulation command can be changed for any duration to represent a range of square power pulses. The SPICE simulation can also be used to investigate the junction temperature for any power profile applied to the diode.

Figure 89 | PMEG050T150EIPD
Cauer model setup in Spice.

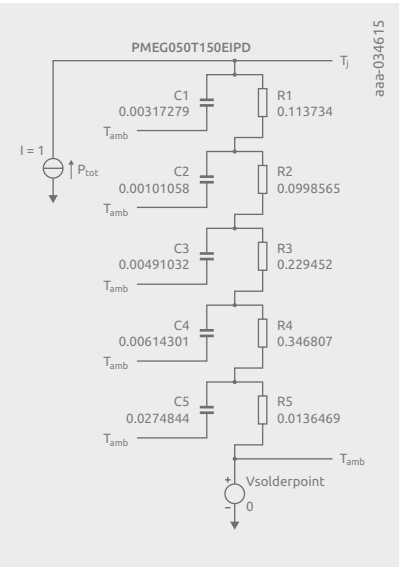
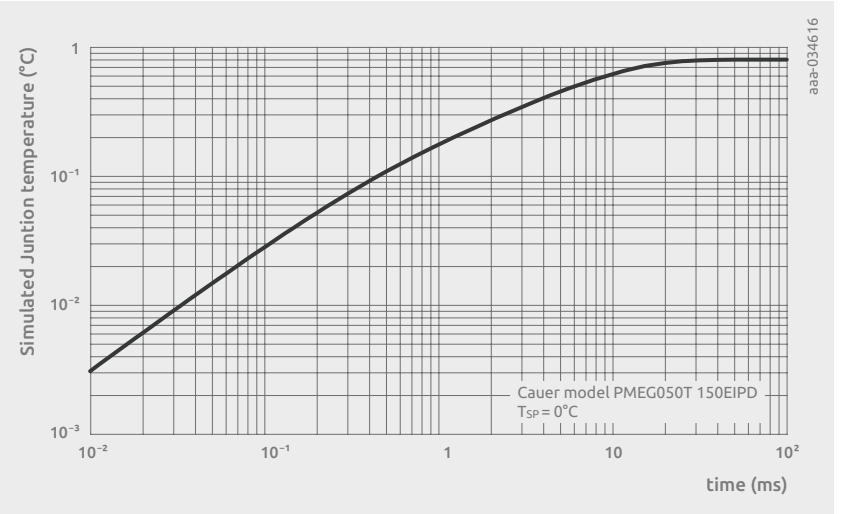


Figure 90 (below) | Simulated junction temperature vs. time for an applied power of 1W to PMEG050T150EIPD. Solder point temperature set at 0°C.



Chapter 5
Diode packaging

Nexperia offers a wide range of packages for diodes, ranging from through-hole packages – a technology which marked the beginning of the mass production of electronics products in the 1950s – to the most modern packages in the industry.

A categorized overview of the Nexperia diode package portfolio is shown in Figure 91.

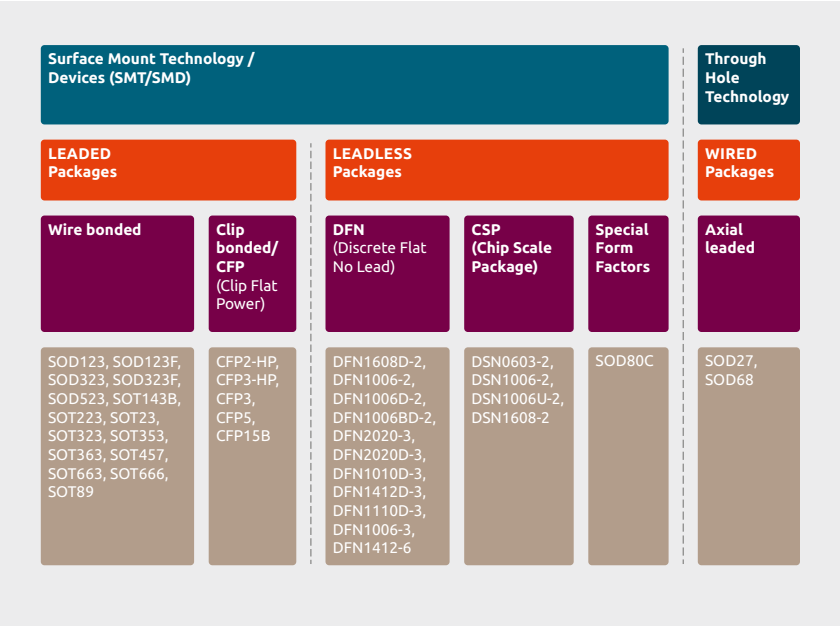


Figure 91 | Categorized overview of Nexperia diode package portfolio.

In the following chapters, package families are presented with their individual benefits in the applications.

5.1 Through-hole packages

From the beginning of the mass production of electronics in the 1950s until the early 1980s through-hole was the standard technology for board mounting. But from the 1980s until today, through-hole has been widely replaced by surface-mount technology (SMT) which opened the way to higher integration and miniaturization. Another reason for the phase-out of through-hole packages was the increasing operating frequencies of electronic applications which made the usage of these packages with their high parasitic inductances – caused by the long leads – undesirable.

But through-hole packages still have advantages in certain circumstances, e.g.

- if large components are required.
- if the space directly on the board is used for surface-mounted devices (SMD) and the through-hole component with its long wires can be placed on a 'second floor'.
- if very tough mechanical stresses and strains need to be considered (e.g. for connectors).
- in special application areas such as power MOSFETs and IGBTs.
- if very simple electronic applications can be realized very cost efficiently by using through-hole technology.

The usual soldering technique for through-hole components is wave soldering. But it is also possible to mount these products using today's common reflow solder lines. Please refer to 4.4 for explanation of different soldering techniques.

5.2 Packages for surface-mounted devices

The introduction of surface-mounted devices in the 1980s into mass production opened the way for the cost-efficient production of ever-more complex electronic applications thanks to the rapid increase of the component density on a PCB. This was enabled by significant and frequent miniaturization steps at component and board level. For the PCBs this meant the steady reduction of the linewidth of the printed-circuit tracks resulting in a massive increase in the line density, and the steady increase in the number of layers in the PCB. Furthermore, the introduction of SMD products opened the way to use both sides of the PCB for mounting devices.

Development of surface-mount technology started in the 1960s. For Nexperia, the era of surface-mounted devices began with the introduction of the famous SOT23 package in 1969 which is still a high-runner in the market.

5.2.1 Wire-bonded leaded packages

Nexperia offers a large variety of wire-bonded leaded-packages. These packages are the correct choice for standard application requirements, i.e. if there are no increased requirements for power, heat dissipation, parasitic inductance or capacitance.

In this package family we find the oldest and most common SMD packages in the discrete semiconductor industry, which still represent the largest volume in the market by number of products sold.

All packages of this category (see Figure 92) are suitable for wave soldering and reflow soldering. The quality of the soldering process can be easily monitored by automated optical inspection (AOI). These packages are qualified for automotive use according to AEC-Q101.

Figure 92 | Table of Nexperia diode leaded-packages with outline and dimensions in mm.

5.2.2 Clip Flat Power (CFP) packages

The CFP-package has been designed for increased requirements in terms of power. The clip bonding which is used in these packages reduces the on-resistance of the product due to enlarged contact areas compared to single wire bonds. Parasitic inductance is reduced thanks to the elimination of the wire bonds. Furthermore, the architecture of the clip bonded packages improves the heat dissipation significantly, making them the preferred choice for power applications.

CFP packages used for Nexperia's diodes (see Figure 93) are all qualified for automotive use according to AEC-Q101 and suitable for wave soldering and reflow soldering.

Due to the high requirements concerning power (temperature) and heat dissipation, clip-bonded packages today (in 2021) still use solder alloys with high lead content for internal package soldering. These solder alloys are used for their unique properties, such as high melting points and high thermal conductivity which ensures the performance and reliability of these packages. Nexperia and other semiconductor manufacturers are working on potential lead-free solutions to replace these alloys to support environmental initiatives.

Figure 93 | Table of Nexperia diode CFP packages with outline and dimensions in mm.

5.3 Leadless packages

5.3.1 Leadframe-based Dual-Flat-No-Leads packages (DFN)

DFN packages are the next significant step in miniaturization. They also offer improved performance in terms of parasitic inductance and capacitance due to shorter wire bonds and no leads. They also show an improved thermal performance by providing one contact pad – or even a large exposed die pad – for direct heat transfer from the silicon to the PCB. The footprints of DFN packages also simplify PCB trace routing.

For a growing part of Nexperia's DFN package portfolio we offer alternative pad architectures with side wettable flanks. These pads are not completely terminated on the bottom side of the product but offer a solderable area on the side wall of the device. This means that after successful reflow soldering, a solder meniscus is visible at the side wall of the device pad. This meniscus can easily be detected using AOI equipment which makes these packages the preferred choice for applications which require extremely high reliability.

The DFN packages for Nexperia's diodes (see Figure 94) are all qualified for automotive use according to AEC-Q101 and suitable for reflow soldering.

Figure 94 | Table of Nexperia diode DFN packages with outline and dimensions in mm.

5.3.2 Chip Scale Packages (CSP)

Nexperia's chip scale packages facilitate electrical functionality on the smallest possible PCB area. The length and height dimensions of the product are the dimensions of the silicon die itself, as the product is basically a naked die with plated contact pads underneath to enable the solder contact to the PCB. Besides minimizing the footprint area, this architecture delivers the lowest values for parasitic inductance and capacitance. This package architecture is called DSN (Discrete Silicon No lead) at Nexperia. Compared to plastic packages, DSN packages require smaller pads and less solder paste to be applied to the PCB for the reflow process. Please take note of the package-related application notes for DSN reflow soldering and footprint recommendations at nexperia.com.

Strongly related to the naked silicon DSN packages are overmolded derivatives offered by Nexperia. These packages are completely encapsulated in a thin layer of mold compound and are listed as DFN packages in the Nexperia package catalog (see Figure 95). But due to the very thin overmolding, these packages are also true chip scale packages as the area ratio between the final product and the encapsulated silicon die is only just below 1.

All chip scale packages can only be mounted using reflow soldering.

Figure 95 | Table of Nexperia diode CSP packages with small sketch and dimensions in mm.

5.4 Soldering techniques

5.4.1 Wave soldering

Wave soldering is the oldest way of mass soldering devices onto PCBs. Wave soldering was introduced when the boards were single-sided and devices used packages with Through-Hole-Technology (THT). The packages had pins or wires which penetrated plated holes in the PCB, and were wave-soldered on the underside of the PCB.

The next evolutionary step was the double-sided PCB with circuitry on both sides of the board. This technology provided enabled SMD packages to be placed on the solder site of the PCB and fixed with glue underneath the package body. These SMD packages and the through-hole packages were then fluxed and soldered using a wave-soldering process.

With advancing miniaturization in PCB and package technology, wave soldering has increasingly been replaced by new soldering techniques, namely reflow soldering. If wave soldering is still required or has its benefits – e.g., for mechanical reasons for connectors or large capacitors – selective wave soldering technologies have been developed which allow the application of a solder wave on very small areas measuring just few square millimeters.

5.4.2 Reflow soldering

With ever-continuing miniaturization, the need for higher and higher pin counts for ICs and the accompanying introduction of new package architectures (e.g., QFN, BGA, chip scale package etc.), wave soldering technology was replaced by reflow soldering which today is the most common way to mass solder devices on PCBs. The fact that modern package architectures use the area underneath the package body for solder contacts means that wave soldering is not an option anymore. Furthermore, the pitch sizes between the contacts have often been reduced to a level which makes reflow soldering a necessity.

Solder paste is printed into the PCB through a mask (stencil). For very advanced requirements or prototyping there are also tools available for direct solder paste printing (dispenser) – comparable to ink jet printers. Solder paste is a suspension of flux and solder powder. It forms the solder joint between PCB pad and device pad after the reflow, and fixes the device after the pick and place process on the PCB before the reflow. If required, a dot of glue underneath the device can be applied on the PCB to support adhesion. The classification of the solder paste (determined by parameters like viscosity and particle size of the solder powder) needs to fit to the PCB and stencil characteristics (minimum pad/hole sizes, stencil thickness etc.).

After solder paste print and device placement, the PCB – with the devices sticking in the solder paste – is driven at a defined speed through the heating zones of a reflow oven. The result of these defined conditions is a temperature-over-time profile which each individual device experiences. For a successful reflow process this temperature profile needs to fulfill certain criteria:

- limits in the rate of heat-up and cool down steps
- limits for the time period above liquidus temperature

The temperature profile depends on many parameters, including the number of PCB layers, the copper density on the PCB, the device size, and its thermal mass to name just a few. It is obvious that the temperature profile will not be the same across the whole board – there will be local differences. Hence, it is important to see that the solder reflow process must be optimized for each individual PCB layout. The semiconductor manufacturer can only specify the range of what the temperature profile should look like for an individual IC or discrete device. The definition of the reflow process is the task of the board manufacturer.

Chapter 6

Reliability aspects

As Nexperia we follow our ZERO quality policy:

- **Z** **ZERO** customer incidents is our ambition
- **E** **EVERYONE** is responsible for quality
- **R** **RECOGNIZED** leadership in quality
- **O** **OBSESSION** for consistent quality

To achieve our ambitions, reliability testing is one of the major considerations during the qualification of our products as well as when monitoring production.

Reliability testing can guarantee that products will perform according to their specifications over the specified lifetimes of the electronic applications.

The parts can fail in the field for a variety of generic reasons:

- Fundamental wear-out mechanism of part (silicon or package)
- Drift in a device parameter
- Latent manufacturing defects
- Manufacturing process excursions

Reliability qualification can address only some of these causes of field failures.

Since reliability qualification is a one-time event, it normally does not address issues such as manufacturing process excursions or 'maverick lots' (maverick lot is an outlier lot which is still within specifications).

Reliability qualification mainly focuses on:

- Detecting fundamental wear-out mechanisms
- Detecting design marginality combined with parameter drift
- Determining failure rates due to latent manufacturing defects

6.1 Probability of failure

Figure 96 shows three different types of failure rates. Early failure rate (EFR), intrinsic failure rate (IFR) and the wear-out period.

The two important periods for the product reliability assessment are Early Failure Rate (EFR) and Intrinsic Failure Rate (IFR). EFR is a declining failure rate. These are failures due to weak products with macroscopic defects. The flat portion of the failure rate curve (IFR) consists of random failures and the failure rate is relatively constant. This is the behavior observed in large populations of mature parts and is commonly referred to as the useful life of the product.

Wear-out is generally not a concern for well-developed semiconductor technologies.

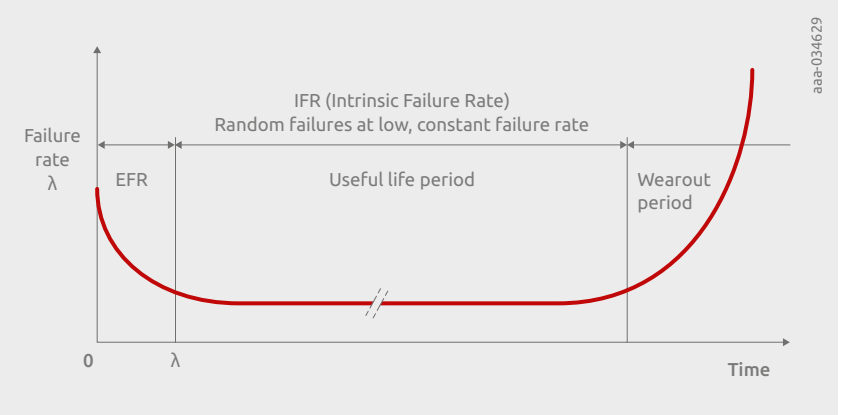


Figure 96: Plot of typical failure rate over time, commonly known as 'bathtub-curve'.

6.2 Reliability tests & failure modes

To check the product reliability before a general release to production, several tests are necessary which focus on a calculated accelerated aging of different parts of the product (die, package & interconnections). Acceleration usually consists of high temperature or a high applied voltage.

We can categorize these tests in different chapters:

- Manufacture
- Operation
- Thermo-Mechanical
- Standby/Storage

Reliability tests – manufacturing & design

Table 24: Reliability tests for investigation of failure modes caused by manufacturing and design.

Test	Explanation	Conditions
Preconditioning	Simulate temperature + humidity prior to reflow solder (defines the moisture sensitivity level (MSL))	24h bake 125°C, 168h H3TRB, 3x reflow
Solderability	Test proper lead finish (tin) to ensure high speed soldering	immerse for 5s in Pb-free solder bath, device may be pre-aged by 8h steam or 16h dry bake
Solder Heat	Test ability to withstand immersion during wave soldering	Immerse in Pb-free solder bath for 30s

Potential failure modes:

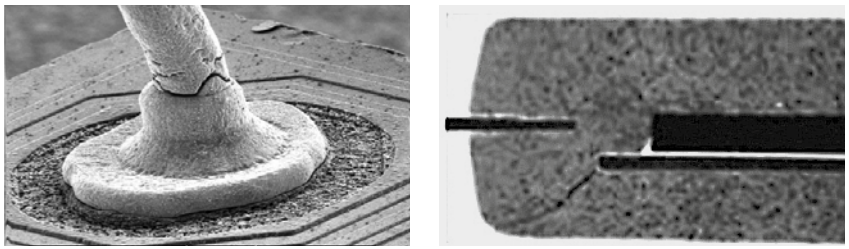


Figure 97 | Potential failure modes might be caused by manufacturing: broken wedge (left), package crack.

Reliability tests – operation

Table 25: Reliability tests for investigation of failure modes caused during operation.

Test	Explanation	Conditions
HTRB	High Temperature Reverse Bias *Acceleration:* Peck model, Temp, V_bias	Oven @ 150°C 1000h max. reverse bias
HTOL	High Temperature Operating Life *Acceleration:* Peck model, Temp, V_bias	Oven @ 150°C 1000h max forward bias

Potential failure modes:

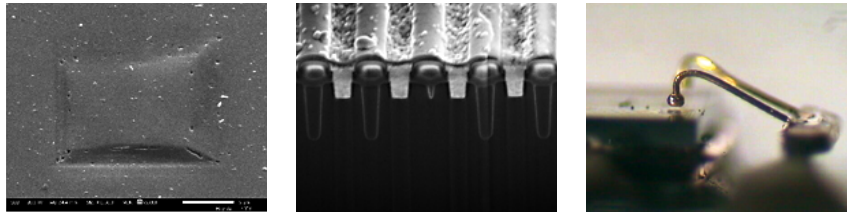


Figure 98 | Potential failure modes during device operation: crystal defects (left), incomplete trench (center) and lifted bond due to intermetallic corrosion.

Reliability tests – thermo-mechanical

Table 26: Reliability tests for investigation of failure modes caused by thermo-mechanical stress.

Test	Explanation	Conditions
TC	Temperature Cycling *Acceleration:* Coffin-Manson, dT	dual climate chamber @ up to −65°C, +150°C device swaps every 20min, 1000cyc
IOL	Intermittent Operational Life *Acceleration:* Coffin-Manson, dT	electr. test rack, device powered on/ off every 2 min, min. temp swing: 100°C (due to Ptot during t_on); 15kcyc
TS	Temperature Shock like TC but with liquid baths	dual climate chamber @ up to −65°C, +150°C

Potential failure modes:

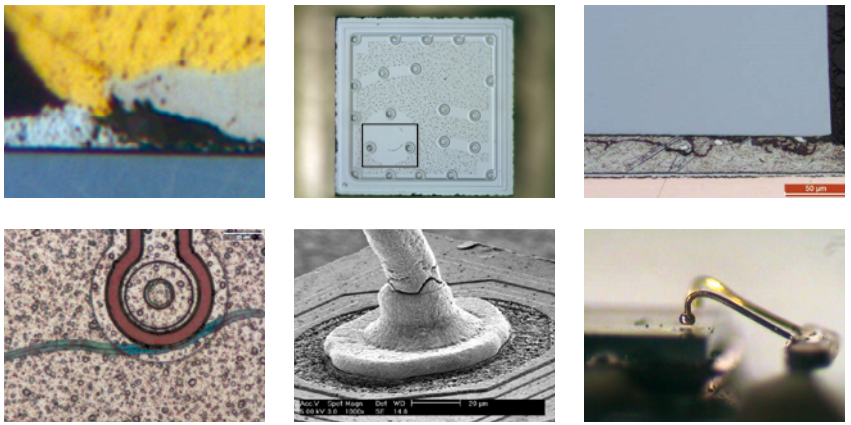


Figure 99 | Potential failure modes caused by thermo-mechanical stress: intermetallic corrosion, cracks in silicon caused by wire bonding, cracks in bond line, cracks in passivation layer, broken stitch, lifted bond wire.

Reliability tests – standby/storage

Table 27: Reliability tests for investigation of failure modes caused by exposure to harsh environment.

Test	Explanation	Conditions
H3TRB	High Humidity/High Temperature Reverse Bias *Acceleration:* Peck model, Temp, %RH, V_bias	climate chamber, 1000h, 85°C, 85%RH, biased at 80% of rated breakdown voltage
AC	Autoclave *Acceleration:* Peck model, Temp, %RH	pressured steam chamber 96h, 121°C, 100%rH, 1bar
UHAST	Highly Accelerated Stress Test *Acceleration:* Peck model, Temp, %RH, unbiased	pressured steam chamber 96h, 130°C, 85%rH, 1.5bar
HAST	Highly Accelerated Stress Test *Acceleration:* Peck model, Temp, %RH, V_bias	pressured steam chamber 96h, 130°C, 85%rH, 1.5bar, biased at 80% of rated voltage

Potential failure modes:

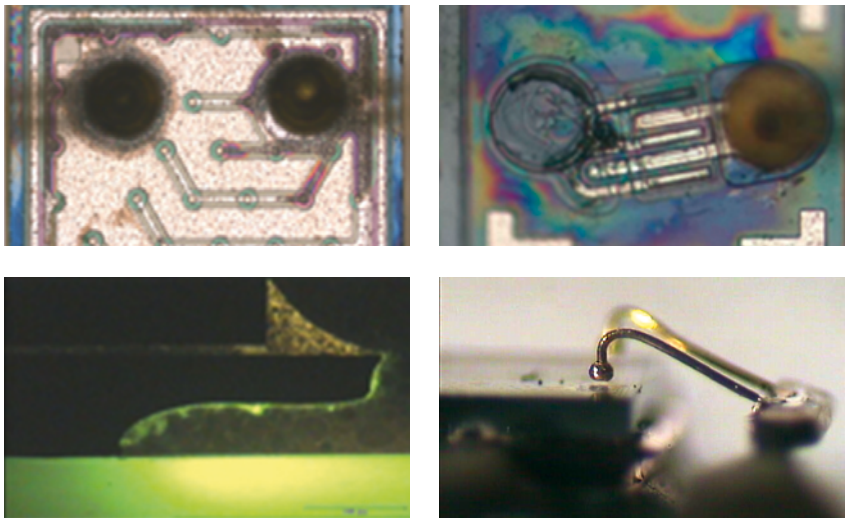


Figure 100 | Potential failure modes caused by exposure to humidity and harsh environment: corrosion (top pictures), lifted bond wire, moisture penetration into package.

During qualification, Nexperia never runs all these listed tests, as some of them cover each other with higher stress levels or extended test duration.

During the setup of Nexperia's qualification strategy, and in parallel to this test selection for a new product family, our company would also consider a structural similarity approach which allows it to perform reliability tests on specific products from the new product family (e.g., smallest and biggest die within a certain family from the same wafer process).

For reliability testing we follow Nexperia's Reliability Qualification Specification as well as the related JEDEC standards for the different tests.

6.3 Automotive-grade qualification

Besides our large consumer/industrial grade qualified portfolio Nexperia has released most of its parts with AEC-Q101 certification, the official automotive qualification guideline.

The difference between the reliability tests for consumer/industrial and automotive products is the test duration (e.g., 500 cycles vs. 1000 cycles TC) which results in a guarantee of longer product lifetime.

6.4 Mission Profiles

A product's intended application area is characterized by a Mission Profile (MP), which is a collection of relevant environmental and functional loads that a product will be exposed to during its full life cycle.

Nexperia uses the following generic Mission Profiles:

- Automotive for Discrete devices, according AEC-Q101
- Automotive, Grade 1 for ICs, according AEC-Q100
- Non-automotive, based on Home Mission Profile from Legacy NXP and on JESD47
- Non-automotive, based on Industrial Mission Profile Legacy NXP and on JESD47
- Non-automotive, based on Infrastructure Mission Profile Legacy NXP and on JESD47

If the customer mission profile deviates from the Generic Mission Profiles, Nexperia is happy to work closely with the customer, to calculate and align on the test conditions and duration to meet the customer's expectations.

6.5 Nexperia's high robustness specification

Nexperia's aim is to produce high-quality products. Therefore, we define our High Robustness Specification accordingly. This document describes the qualification requirements for products to be released as 'High Robustness Products' – products which are used in extreme automotive customer applications such as Engine Control Units or gear boxes.

On top of AEC-Q101 we add some very ambitious tests:

2x AEC-Q101:
The test time of all reliability tests according to AEC-Q101 or -Q100 (whichever is applicable) must be extended by the factor of 2.

Zero delamination:
The products must not show any sign of delamination of the mold compound from any other component of the device (e.g., leadframe, clip, wire, die) after pre-conditioning according to MSL 1.

PCB bending test:
The products must withstand at least 1.0mm of PCB bending according to IEC-60068-2-21. In addition, the maximum possible bending deflection before the parts fail electrically must be determined.

Vibration test:
A vibration test in accordance with IEC60068-2, 64 using the specified conditions must be passed.

Drop test:
A drop test using the following conditions must be performed: pulse width (measured at 10% of amplitude): 0.5ms +/-30%, Cpk>1.33, acc. peak 1500g +/-20%, Cpk>1.33 (see picture). The samples are monitored electrically throughout the test. The number of samples to be tested are 135 per (leader-)type, distributed on 9 test boards.

Power thermal cycling:
The PTC test is a combination of TC and IOL which leads to a high stress at the interconnection between PCB and Product. 2600 PTC test cycles are required.

- TCT condition: –40°C to 105°C, 90min/cycle
- IOL condition: Seven powered component cycles (5 minutes on, 5 minutes off) with a temperature rise of 30K ± 2K between solder joint of the component on the PCB and an aluminum base plate attached to the PCB are required.

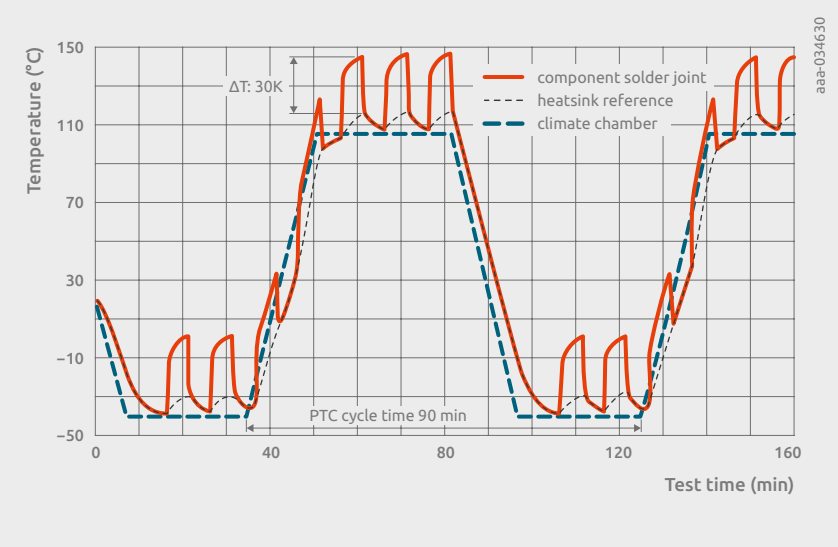


Figure 101 | Power temperature cycling. Power temperature cycling is a very specific test combining TC and IOL which leads to a high stress at the interconnection (solder joints) between PCB and Product.

For any questions about Nexperia's qualification strategy don't hesitate to get in touch with us.

Chapter 7

Diode applications and use cases

7.1 Polarity protection diode

After changing the battery, or during maintenance, the battery leads may be reconnected in the opposite polarity. Wrong polarity of the battery can potentially lead to fatal errors in the electronic units of a vehicle. Therefore, a measure is necessary to protect the sensitive electronic system from reverse battery protection.

Using a diode in series in the supply line can be considered as the simplest and most cost-efficient way to realize a reverse battery protection circuit, as shown in Figure 102.

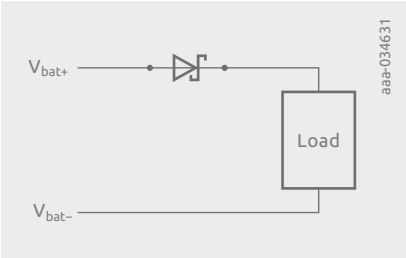


Figure 102 | Reverse battery protection by using a diode in series in the supply line.

The steady state conduction losses P_{loss} can be easily calculated by taking into account the forward voltage drop V_f of the diode at a given temperature and the load current I_{load}:

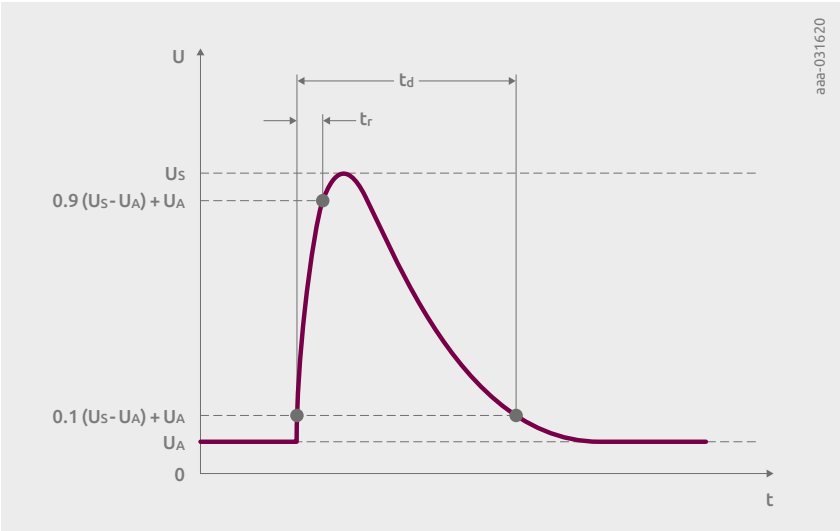
$$P_{loss} = I_{load} \times V_f(T)$$

It is obvious from this equation that a diode for reverse polarity protection is useful for relatively small load currents only, otherwise the power dissipation increases too much, adversely affecting the efficiency of the system. In practice, therefore, diodes are used as reverse polarity protection for load currents up to approximately 2–3A.

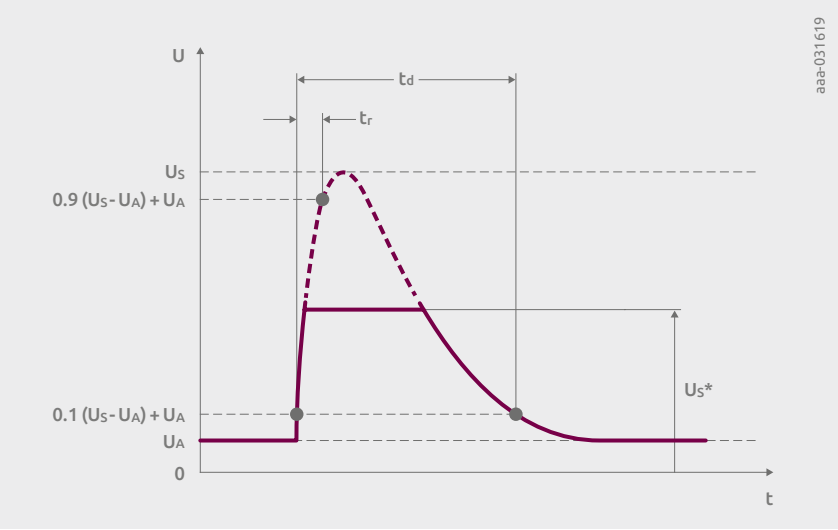
Apart from the power dissipation that the diode must be able to dissipate in the given package, there are other aspects that must be taken into account. These are discussed below.

Load dump

Load dump describes the condition that occurs when the alternator is charging the battery and the connection to the battery is suddenly lost while other loads remain connected. ISO 16750-2 and ISO 7637-2 (Figure 103) specify automotive load dump transients for 12V & 24V systems. According to these standards, the surge transients can last up to 400ms. Normally the reverse protection diode is preceded by a TVS diode which clamps the voltage level of the transient. Nevertheless, the voltage transient can cause a high peak current through the internal resistance of the alternator and the dynamic resistance of the diode. Therefore it is necessary to choose diodes with a high surge current capability for reverse battery protection. Keep in mind that the surge current capability of the diode is specified through the I_{FSM} parameter which is usually defined for rectangular and sinusoidal pulse forms for a pulse width in the range of 8ms, while a load dump peak current can last up to 400ms,– much longer. The choice of the reverse polarity protection diode must be decided on a case-by-case basis, considering the pulse duration, the selected TVS diode and the internal resistance of the alternator. However, it can be generally recommended to use a diode in a clip-bonded package, such as the Clip-bonded Flatpower (CFP) package family from Nexperia, as such products come with a significantly larger surge current capability thanks to the use of a solid copper clip.



Board net	U_s (V)	R_i (Ω)	i_d (ms)	t_r (ms)
12V	65 to 87	0.5 to 4	40 to 400	10 +0/-5
24V	123 to 174	1 to 8	100 to 350	10 +0/-5



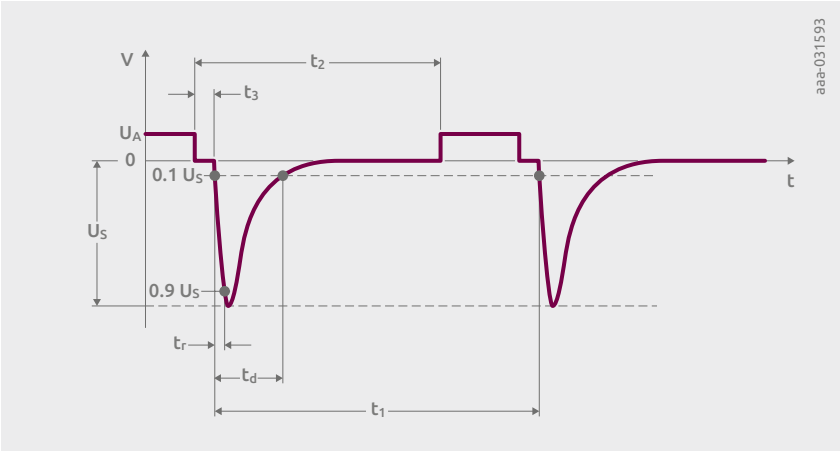
Board net	U_s (V)	U_s* (V)	Ria (Ω)	t_d (ms)	T3 (ms)
12V	79 to 101	35	0.5 to 4	40 to 400	5 to 10
24V	151 to 202	Not specified	1 to 8	100 to 350	5 to 10

Figure 103 | Test pulses for characterizing the load dump transients.
Left: unsuppressed transient, right: suppressed transient.

Battery disconnection from an inductive load

ISO 7637-2 also describes what happens when the connection to the battery is interrupted while an inductive load is applied in parallel with other loads. The inductive load will generate a negative voltage across the loads. This condition is tested according the test pulse shown in Figure 104.

As shown in the table, the reverse peak voltage applied to the anode of the diode can be up to −100V for a 12V board net. The diode must be designed in such a way that the dissipated power in the reverse direction on the time scale of the pulse does not exceed the specified avalanche energy of the diode. Another important point to consider is the leakage current of the diode. Especially at high ambient temperatures, the diode will carry a leakage current that can stress the sensitive load. Therefore some designers use recovery rectifiers instead of Schottky diodes in order to control the leakage current. However, due to the pn junction, recovery rectifiers have a high forward voltage drop, compromising the efficiency of the reverse polartiy circuit. This is where SiGe diodes can help. This new hybrid technology combines the advantages of Schottky diodes with the low leakage current of recovery rectifiers. Please refer to chapter 1 for more details.



Board net	U_a (V)	U_s (V)	R_i (Ω)	t_d (ms)	t_r (µs)	t1 (s)	t2 (ms)	t3 (us)
12V	13.5 ± 0.5	−75 to −150	10	2	0.5 to 1	> 0.5	200	< 100
24V	27 ± 0.5	−300 to −600	50	1	1.5 to 3	> 0.5	200	< 100

Figure 104 | Test pulse for characterizing transients caused by the disconnection of batterie from an inductive load.

7.2 Zener applications

Zener diodes are often used to generate a stabilized voltage. In Figure 105 a Zener diode ZD1 is connected to a voltage source via a series resistor. The load resistor R_{LOAD} is connected in parallel to the Zener diode. This load could also be a sophisticated electronic circuit requiring a stable supply voltage.

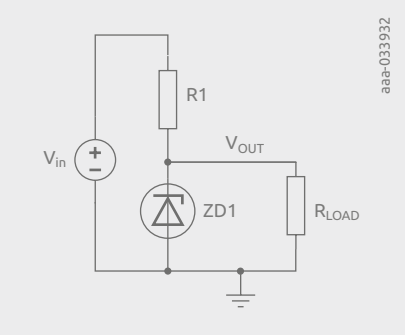


Figure 105 | Voltage Stabilizer with a Zener diode.

The value of series resistor R1 has to be chosen such that residual current flows through the Zener diode also for the highest load current that may be expected. The minimum current through the Zener diode should ensure that the diode operates in the steep region of reverse conduction. The current used for the measurement of V_Z in the datasheet is a good guide, this means about 5mA for values of V_Z up to 17V and 2mA for Zener diodes with high Zener voltages.

$$R1 = \frac{V_{IN} - V_Z}{I_{Z(min)} + I_{LOAD(max)}}$$

The power dissipated in R1 is:

$$P_{R1} = \frac{(V_{IN} - V_Z)^2}{R1}$$

The Zener diode has maximum power dissipation if no load is connected. In this case, all the current via R1 flows through the diode:

$$P_{ZD1} = V_Z \times I_Z = V_Z \times \frac{V_{IN} - V_Z}{R1}$$

The basic voltage stabilizer circuit shown in Figure 105 is used for low power requirements. For load circuits with a higher power requirement, it is not efficient that the full current through R1 heats up the Zener diode when the load is turned off, or that so much heat is generated if load current consumption drops during use. The circuit in Figure 106 improves this significantly. The Zener diode ZD1 is driven in breakdown via R1. The base of the bipolar transistor Q1 is connected to the stabilized voltage across ZD1. The output voltage at R_{LOAD} is determined according to the equation: $V_{OUT} = V_Z - V_{BE}$.

Power dissipation in the Zener diode is almost independent from the load current if it is assumed that the base current is only a small part of the current through R1. For output voltages of about 5V, the circuit has quite a good thermal stability because the thermal coefficient of the Zener voltage of about −2.0mV/K is compensated for by a decrease of V_{BE} with a very similar coefficient.

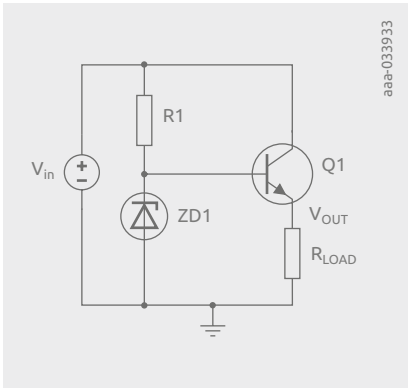


Figure 106 | Voltage Stabilizer with a bipolar transistor and Zener diode voltage reference.

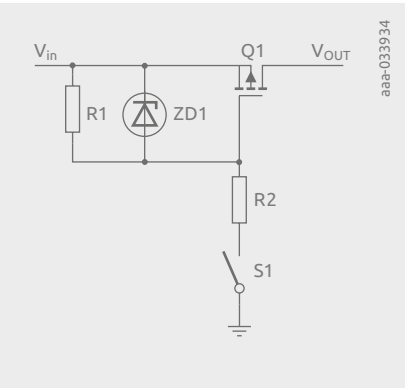


Figure 107 | Load switch with P-Channel FET and Zener diode for gate voltage clamping.

Another important application for Zener diodes is the clamping of undesired over-voltages. In Figure 107 a simple load switch is depicted. The gate oxide of MOSFETs is sensitive to over-voltages. Internal ESD diodes of FETs should not be used for clamping in an application because the gate-source voltage V_{GS} is above datasheet limits in this case. The breakdown voltage of the ESD diode is higher than the specified V_{GS}-rating. In the application example a P-channel FET switches the load current. The FET turns on once the gate has a negative voltage versus the source. If switch S1 is turned on, the voltage divider of R2 and R1 with ZD1 in parallel define the gate voltage to be higher than $V_{GS(th)}$. The voltage at the gate is limited by ZD1 to a level which is within the V_{GS} rating of the FET with some safety margin. The gate voltage can be adjusted by a resistor divider without a Zener diode. However, in this case, the circuit is not safe if V_{IN} sees over-voltage events.

The resistor R1 has to be applied for discharge of the gate once the load switch is turned off. S1 is usually realized using an N-channel control FET or a BJT.

Figure 108 is another solution for protecting a MOSFET. The FET Q1 is switching an inductive load. The inductance has no free-wheeling diode. Once the switch turns off, the current continues to flow. L1 creates a voltage which is high enough to break through the drain-source path of the FET. However, with the Zener diode applied between the drain and gate of the FET, the FET can switch on again slightly so that the V_{DS} rating is not exceeded. The FET runs in linear mode for a short duration and the energy stored in the inductor is dissipated in the FET in a comparably short time. Compared to a simple free-wheeling diode parallel to L1, a higher voltage loss across the drain-source path leads to higher power and faster decay of the stored energy in the inductor.

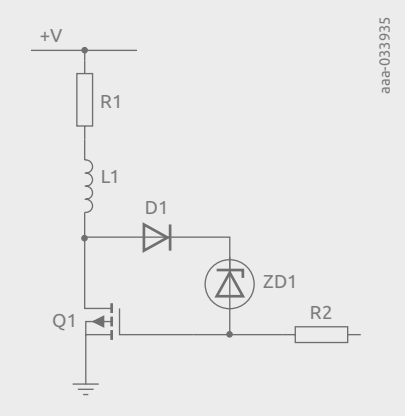


Figure 108 | Protection of a switch for an inductive load with a Zener diode.

Zener diodes can be used for all kind of applications where voltage levels have to be clamped or kept below a limit. Figure 109 shows a level limiter for an AC source. For a sine wave source the maxima and minima are symmetrically clipped to $V_Z + V_F$.

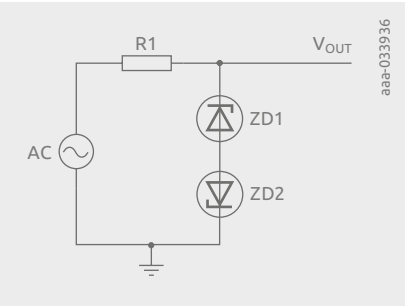


Figure 109 | Example for level clipping of AC voltage by Zener diodes.

Figure 110 is a SPICE simulation result of a 1kHz sine wave voltage source supplied through a 220 ohm resistance to two Zener diodes with a V_Z of 5.6V. The two Zener diodes are connected in series with their anodes connected (as shown in Figure 109). It can be seen that the clipping levels are about 0.6V higher than V_Z, as can be expected. Using a similar approach, Zener diodes are often implemented for ESD and surge pulse protection of signal lines. With the voltage clipping function they prevent excessive over-voltages that could endanger and damage electronic circuits.

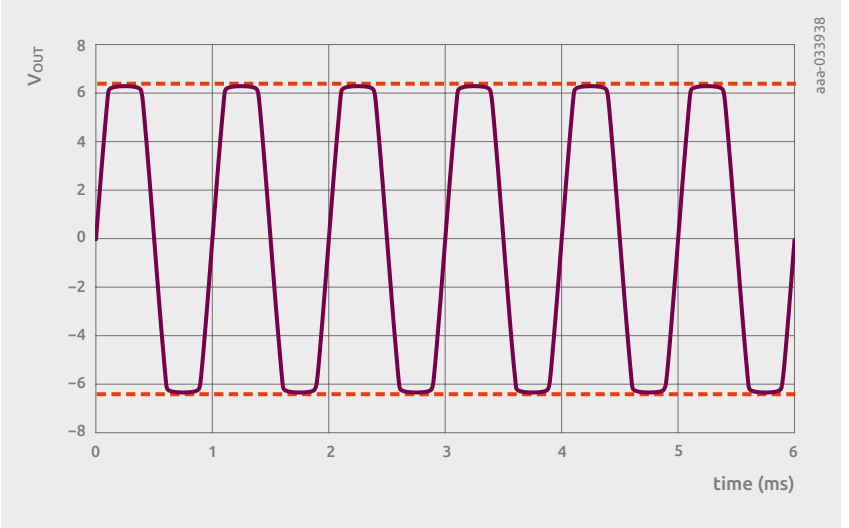


Figure 110 | Symmetrical clipping of 1 kHz sine wave with BZT52H-B5V6.

Zener diodes are often used as voltage references. Figure 109 shows an example where an op-amp is used as a non-inverting buffer to provide the reference voltage created by the Zener diode ZD1 as an output voltage with low impedance for the connected electronic loads. The current through the Zener diode can be chosen to be small compared to the circuit shown in Figure 105. In order to support such applications with a narrow spread of V_Z at low Zener currents, dedicated low current Zener diode families are offered. Instead of the 5mA current rating used for standard Zener diodes, these components are rated for 50µA. If standard Zener diodes are used for low current applications, the parts should be tested upfront, in order that clamping works as desired.

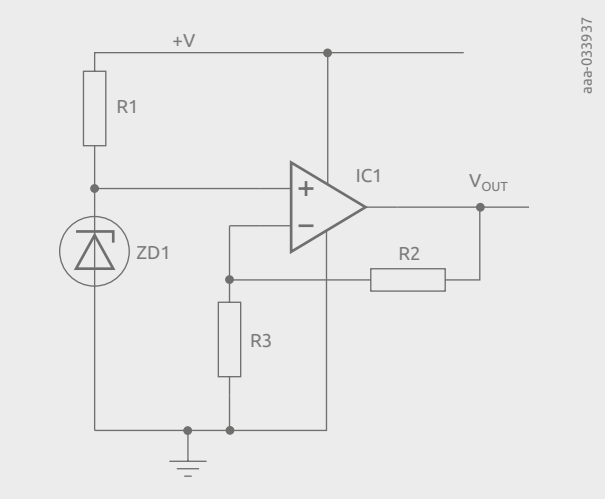


Figure 111
Zener diode as voltage reference with an Op-Amp buffer.

Irrespective of the chosen supplier, it can happen that at certain special Zener voltages the avalanche effect can be observed with some delay. Therefore, noise as shown in Figure 112 can occur for a very small current I_Z. If the Zener diode crystals are doped with gold or platinum, these impurities can deliver the necessary carriers for avalanche breakdown at low bias currents. This ensures that an avalanche breakdown happens safely and accurately, even with low avalanche currents.

As an experiment to check the reliable operation of Zener diodes at low currents, a high impedance, say 1MΩ, can be put in series with the Zener. A low current created by a current source is pushed through the diode while V_Z is tested using an oscilloscope. Figure 112 shows the example of such undesired behavior.

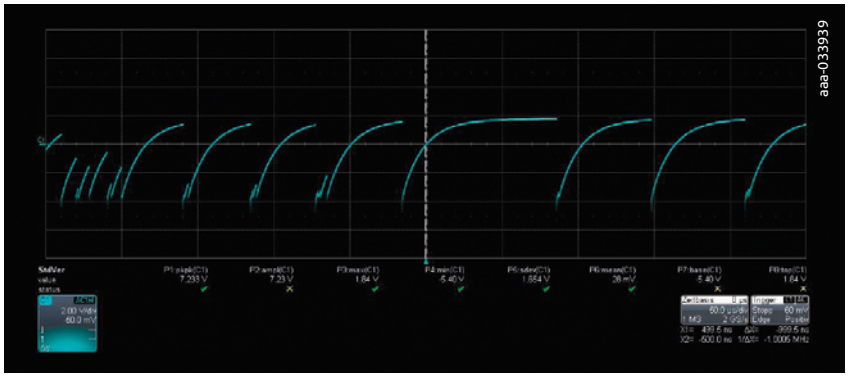


Figure 112 | V_Z of a 75V Zener diode with I_Z = 30µA supplied via a 1MW impedance, showing unstable avalanche events.

7.3 ORing applications

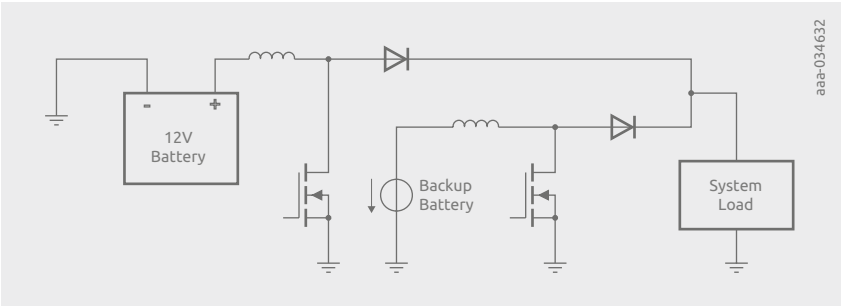


Figure 113 | Diagram of a system with two power sources for increased safety through supply redundancy. The main power source and the backup battery are isolated from each other by two ORing diodes.

In systems that have to meet high safety requirements, a power architecture with redundancy is mandatory. An example of this is the emergency call system in a car. In such a case, at least two power supplies are connected to the load. There is a main power supply and a back-up battery as shown in Figure 113. Diodes are used to isolate the two power supplies from each other. Very similar to the case of reverse polarity protection, diodes are a simple and cost-efficient solution for power supply redundancy applications. However, due to the relatively high power losses in the diode, diodes are only suitable for small currents. In order to keep these losses low, Schottky diodes usually preferred, since they have a smaller forward voltage drop compared to diodes with a pn junction. Another requirement is a low reverse leakage current, even at high ambient temperatures. The reason for this requirement is because the two power supplies don't necessarily have the same voltage levels, which means that one diode will be biased in reverse. The leakage current of the diode would then by fed into the back-up battery which could potentially cause damage to the battery.

Here, again, the I_R/V_F trade-off of diodes comes into play. Nexperia offers a whole range of Schottky diodes with low reverse leakage current in different packages. If very low reverse leakage currents at high ambient temperatures are required, SiGe diodes can also be used here, as they exhibit relatively low forward voltage drops despite their extremely low reverse leakage current.

7.4 Switching diode

Switching diodes can be found in nearly every electronic application. In this section, some examples are discussed that can be found in many applications.

Switching diodes can be used in extremely low cost solutions for simple, slow-speed logic functions as depicted in Figure 114. The control signals S1 and S2 are connected via two diodes to a resistor R1. Once at least one signal has a positive voltage level significantly above V_F, a current will flow through R1. If we see the simple circuit as a logic function, an OR-gate is created. There is a positive voltage at R1 if one input signal, S1 or S2, or both, get a positive input voltage. The circuit can be extended easily to connect more control signals in this way by adding more diodes.

The diodes decouple the input signals from each other. If one signal shows a logic-high state, no current will flow back into the other signals with a logic-low state. If this circuit is connected to a switching stage, such as a BJT or FET, many types of actuators and loads can be controlled. These can work with different voltages than the input signals S1 and S2.

Figure 115 depicts such a situation. Q1 switches a load resistor R_{load}. The load supply voltage can be chosen without constraints if a suitable FET is selected. The voltage at the drain pin can be seen as the inverted signal of the voltage at R1. The OR-gate created by the diodes is followed by an inverter, so a NOR-gate has been built.

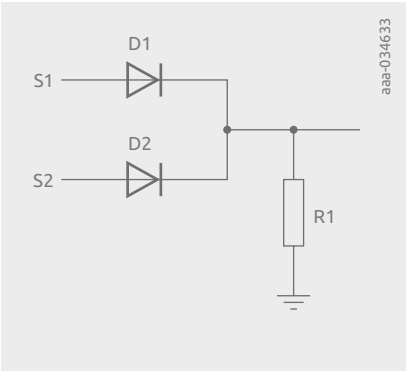


Figure 114 | Diodes used for a logic-OR function.

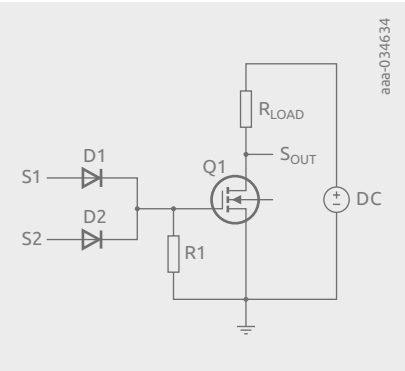


Figure 115 | Diode's OR function extended with FET switch added.

If the switching diodes are connected in reverse compared to Figure 114, i.e. with common anodes at the node S_{out} as shown in Figure 116, the voltage at R1 is V_F, once at least one input has ground level. If all inputs provide a logic-high state, the voltage of the signal S_{out} will also provide a logic high state. The circuit discussed provides an AND function. Again, it can be expanded for a higher number of inputs by adding more diodes. Adding a FET with a threshold voltage above V_F provides the option to switch various loads, and the drain signal has a clean low level if the approach is used as NAND function. Signal S_{out} in Figure 117 can then be used as proper control signal for further circuitry.

The AND function is often used if several control signals have to be present with a positive voltage, all at the same time. There may be several switches safeguarding the proper condition of a system – for example, all doors closed – and some supply voltages may be mandatory to enable a further operation.

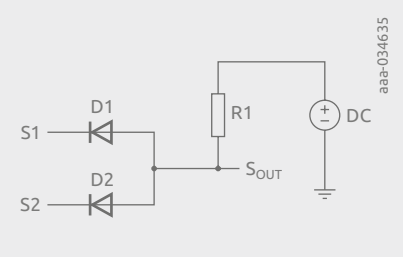


Figure 116 | Diodes AND function.

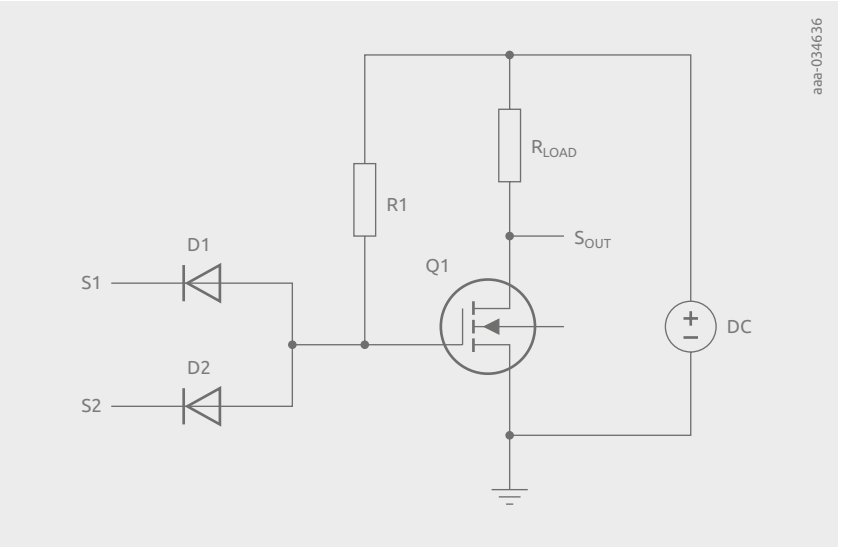


Figure 117 | Diodes AND function with FET switch added

Switching diodes are often used for voltage clamping in a rail-to-rail approach. Figure 118 depicts this solution. If a negative voltage surge pulse against ground level enters the system, the low side diode becomes conductive and clamps the voltage of signal S1 to $-V_F$. For positive surge events, the upper diode starts to conduct once the voltage exceeds $V_{CC} + V_F$. Usually, big capacitors are connected to the supply line, called V_{CC} in the example, and the impedance of the line is often quite low, with many loads connected. Therefore, voltage V_{CC} will not increase much as a result of an ESD strike which does not have high energy. If higher energy pulses and long duration over-voltage pulses can be expected, a Zener or TVS diode can be added in reverse direction to the supply. In Figure 118 the TVS diode is shown connected with dashed lines, and the over-voltage is limited to $V_{BR} + V_F$. V_{BR} is the breakdown voltage of the Zener diode and V_F is the forward voltage drop of the upper switching diode in Figure 118.

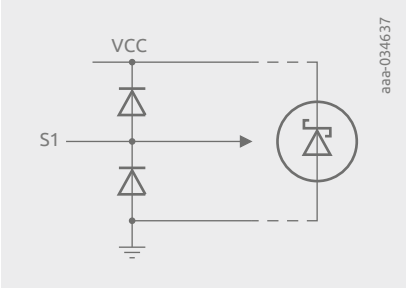


Figure 118 | Switching diodes applied as input protection.

Charge pumps, created with capacitors for energy storage and diodes as switching elements, are another application example for switching diodes. In applications with operational amplifiers, a negative supply voltage is very often required in order to use the ground as reference for the amplifier, rather than a resistor divider in a single supply design. Figure 119 shows a voltage inverter. The oscillator toggles between GND level and a voltage V_1. If the output of the oscillator outputs the positive voltage V_1, C1 gets charged to V_1-V_F via D1. The positive pole of the charged capacitor is then connected to ground once the voltage source switches to GND. By this switching event there is now a negative voltage against ground at the minus pole of the capacitor. Diode D1 is reverse-biased and does not conduct. D2, however, is biased in the positive direction, so C2 gets charged with a negative voltage against GND. With the next oscillator cycle, D2 blocks a discharge of C2 and C1 gets recharged via D1. V_{OUT} is the inverted positive voltage from the oscillator, reduced by the forward voltage losses of the two diodes, so $V_{OUT} = V_1 - 2 \times V_F$.

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The capacitors must be specified with a capacitance that is high enough to achieve a maximum ripple voltage target on V_{OUT}. The values depend on switching frequency and maximum load current.

Figure 119
Voltage inverter with charge pump approach.

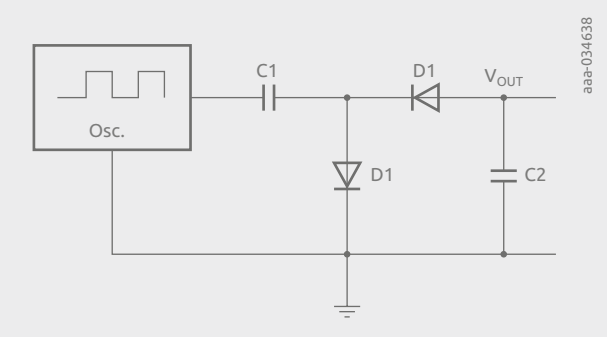

Figure 120 depicts a charge pump circuit which can double the supply voltage. There is a DC supply V_1 and an oscillator that is assumed to toggle between ground level and a positive voltage V_1. If the oscillator outputs ground level, C1 is charged to V_1-V_F. C2 also gets charged to $V_1 - 2 \times V_F$. Once the oscillator toggles to the output voltage V_1, the negative pole of the charged C1 is moved up by V_1, so charge can flow from C1 into C2 increasing the output voltage.

For V_{OUT} there is the equation: $V_{OUT} = 2 \times V_1 - 4 \times V_F$.

The circuit for voltage doubling can be extended with additional stages, so that an input voltage can be multiplied by a factor N, assuming we neglect the forward voltage losses of the diodes.

Figure 120
Voltage doubling circuit with charge pump approach.

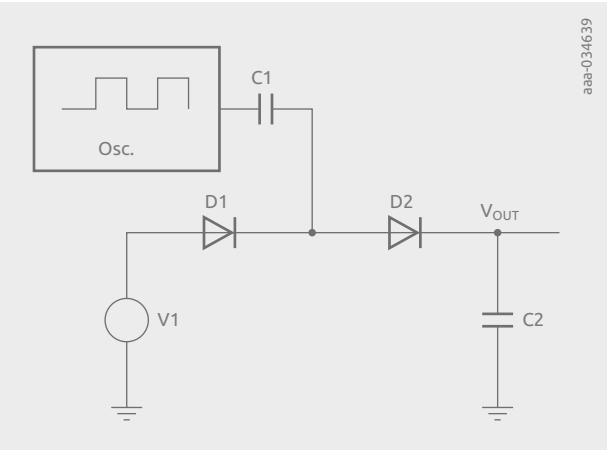

Figure 121 shows a simple peak voltage detector. There is an AC source rectified by the diode D1. C2 is charged to the positive peak voltage of the incoming signal, reduced by V_F. The circuit works as a peak voltage detector. Via a discharge resistor R1, C2 is discharged again, and does not remain forever at the highest voltage ever applied. With an RC time constant $\tau = R1 \times C1$, a discharge of C1 can be achieved. With a time constant chosen significantly higher than the duration T_{in} of one single oscillation in the input signal, an AM demodulator is built. The amplitude of the input signal must be significantly bigger than V_F of the switching diode. For the AM demodulation, the carrier signal should not fall below, or close to, V_F.

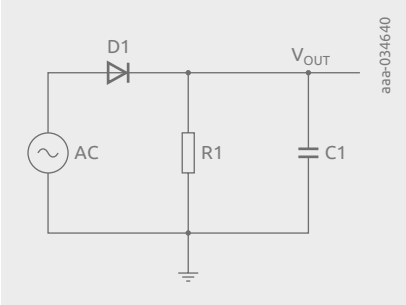

Figure 121 | Peak voltage detector, AM-demodulator.

This disadvantage of the simple circuit depicted in Figure 121 is solved with the more sophisticated approach shown in Figure 122. The positive input of an operational amplifier is connected to the AC source. The output is connected to a diode and directly coupled back to the negative input from the cathode side. C1 is then charged to exactly the positive peak voltage of the input signal. Negative polarity input voltages let the operational amplifier clip at the maximum negative output voltage. The diode blocks this voltage, so the voltage at C1 is not hampered.

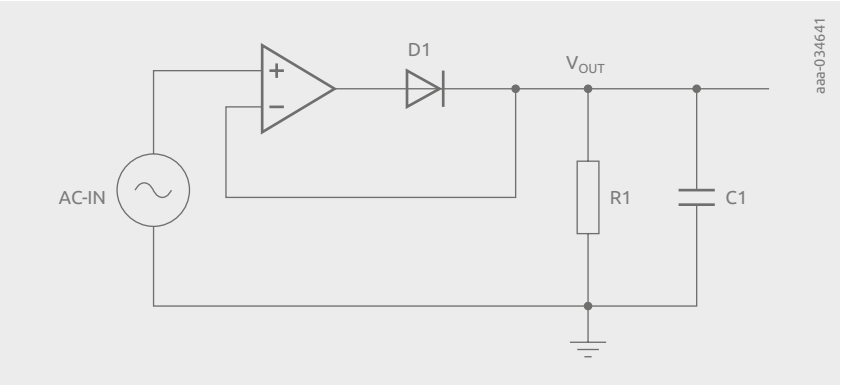

Figure 122 | Precision peak voltage detector.

7.5 Bootstrap diode

Another typical application of switching diodes can be found in the bootstrap circuit, a common way to supply the high-side gate driver in half-bridge circuits. The bootstrap circuit as depicted in Figure 123 is comprised of the bootstrap diode D_{boot} for voltage blocking, a current limiting resistor R_{boot} and the capacitance C_{boot} for energy storage. It is a low-cost alternative to isolated supplies for both low- and high-voltage applications. While some integrated circuits for half-bridge applications already include an integrated diode, a discrete component solution can be used for virtually any half-bridge design, leaving the circuit designer with a maximum degree of freedom.

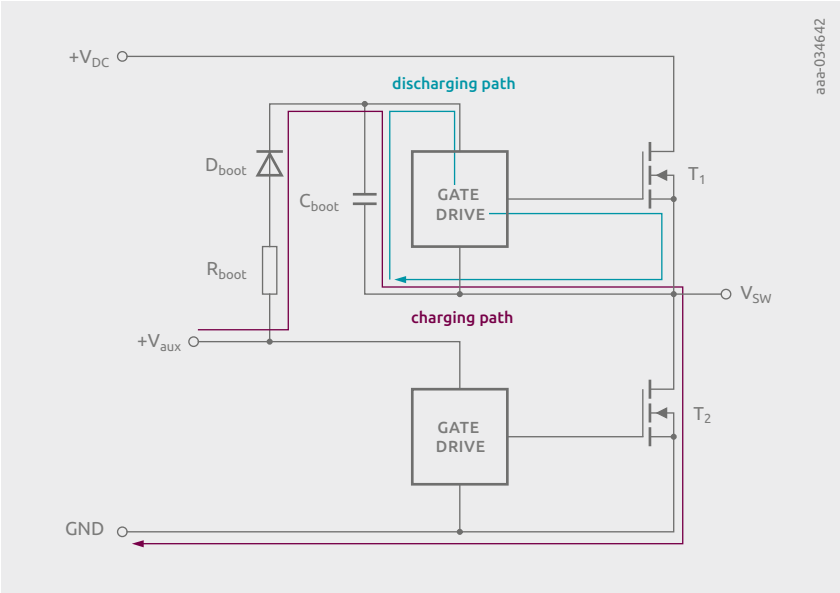

Figure 123 | Half-bridge with bootstrap circuit for high-side gate drive supply.

As illustrated in Figure 123, there are two main states. While the low-side (LS) transistor T_2 is on, the switch-node of the half-bridge is pulled close to the ground potential (GND) and C_{boot} is charged through R_{boot} and D_{boot} by the auxiliary supply voltage V_{aux}. As soon as the low-side FET turns off and the high-side (HS) FET T_1 turns on, V_{sw} is pulled to the HV supply voltage V_{DC} and the bootstrap diode will start blocking. In this state, the high-side gate circuit is separated from the supply rails and will only be powered by the bootstrap capacitor.

Although the bootstrap circuit consists of only three components, very careful selection of each component is important for good performance of the entire half-bridge. The following section is intended to provide an overview of typical design considerations when choosing a bootstrap diode.

Blocking voltage

The bootstrap diode must be designed for the same blocking voltage as the half-bridge FETs. It must be able to block the static HV supply voltage V_{DC} plus any additional turn-off overshoot during operation of the half-bridge circuit.

Dynamic vs. static performance

Both the dynamic switching and the static conducting properties must be considered carefully and a trade-off is often required when selecting the bootstrap diode. In lower frequency designs switching up to tens of kHz, the dynamic properties of fast modern diodes are usually sufficient and a device with low V_F and low leakage can be selected. However, for high-frequency, fast-switching applications, choosing a small diode with low junction capacitance C_j and best possible reverse recovery properties (minimal t_{rr} and Q_{rr}) is mandatory. The stored charge on the diode will be moved on and off during each switching cycle and can lead to considerable losses in R_{boot} at high frequency. In very high frequency designs, the charging current in the bootstrap diode might not decay to zero before the low-side FET T_2 is turned off and reverse-recovery will occur. During this operation, an additional charge Q_{rr} is transferred back from the high-side capacitor during turn-off. This increases the total required charging current, as shown in the comparison between a hyperfast silicon diode and a silicon-carbide MPS (Merged PIN Schottky – please refer to chapter 1.6) diode in Figure 124. In addition, snappy diode recovery can lead to strong ringing that might cause EMI problems, and can even trigger the UVLO protection of the gate drive circuit. For these reasons, Schottky diodes can be a good choice for high frequency designs, even though their static stored charge is usually larger than that of comparably rated p(i) n-diodes.

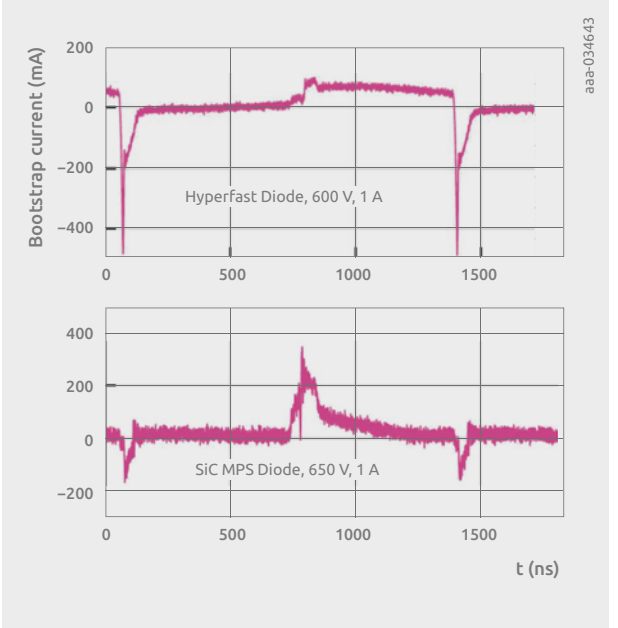

Figure 124
Bootstrap current waveform of Si and SiC bootstrap diodes in a 400V, 750kHz half-bridge circuit.

As a drawback, the small diode will have a lower current capability and higher forward voltage drop V_F. The forward voltage V_F directly impacts the amplitude of the high-side gate drive voltage V_{Cboot}. As shown in Figure 123, C_{boot} is connected to V_{aux} during the charging phase via R_{boot} and D_{boot} leading to the voltage equation

$$V_{Cboot} = V_{aux} - V_F - R_{boot} \cdot i_{boot}$$

For low-frequency designs, the charging time constant $\tau_{boot} = C_{boot} \cdot R_{boot}$ is typically considerably lower than the conduction time of the low-side transistor T_2, as long as the circuit is not operated at very small duty cycles. This allows i_{boot} to decay to 0 and V_{Cboot} will mostly depend on the forward voltage drop of the diode at very low current. In low-voltage designs, the use of a Si-Schottky diode with its very low forward voltage drop can therefore ensure that the high-side gate supply voltage is very close to V_{aux}. In contrast, at high switching frequency and in high-voltage designs, V_{Cboot} can drop significantly below V_{aux}. Both HV p(i)n-diodes and SiC Schottky diodes show significantly higher forward voltage drop and the bootstrap current in high-frequency operation might not decay to zero, leading to additional voltage drop across R_{boot}. Figure 125 shows the results of an LTSpice simulation of a 400V converter operated at a high switching frequency of 500kHz with three

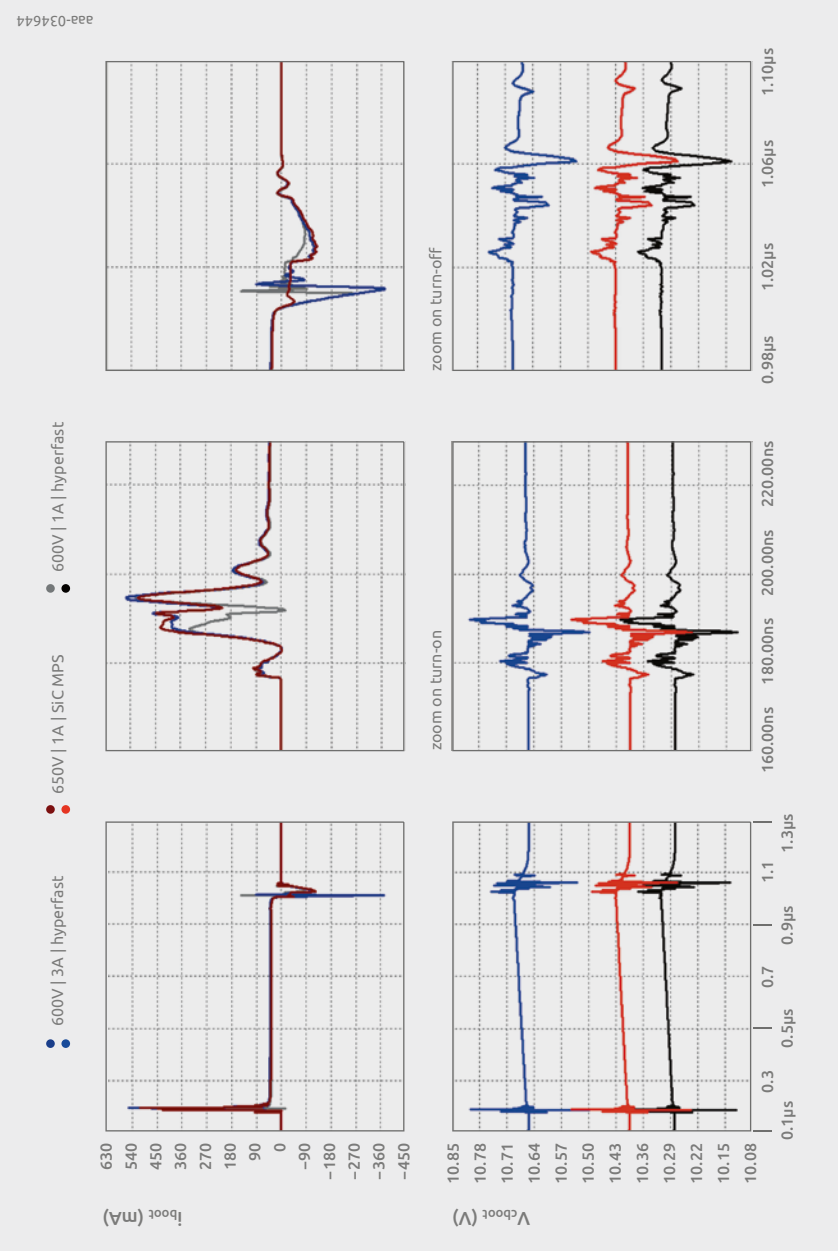

Figure 125 | Simulated waveforms (LTSpice) at 500kHz for different diode types, C_{boot} = 1µF, R_{boot} = 10Ω, V_{aux} = 12V.

different bootstrap diode models. It can be seen that the forward characteristics of the diodes have direct impact on the high-side supply voltage V_{Cboot}, and thus might influence the switching performance of the HS FET. The zoomed turn-on and turn-off current waveforms of the bootstrap diodes in Figure 125 also show the impact of the stored charge on the diodes. The 1A hyperfast diode has the smallest static charge but still leads to lowest HS supply voltage due to its larger V_F drop. Since charging currents do not decay to zero in this scenario, both silicon diodes show reverse recovery. It must be noted that most available diode models for LTSpice might not properly simulate reverse-recovery and thus a measurement is always advisable for these very high frequency converter designs.

Current ratings

As part of the start-up routine in bootstrap powered half-bridges, the low-side transistor is turned on constantly to charge up the bootstrap capacitor C_{boot} on the high-side. The peak current handling capability of the bootstrap diode must be sufficient to support the first current pulse with a peak value of $\hat{i}_{boot} = (V_{aux} - V_F)/R_{boot}$.

This is usually more of a challenge in low-frequency designs with larger C_{boot} since peak duration is longer. In continuous operation, the current requirement is usually many times lower when only the driving losses of the HS FET need to be covered. Nevertheless, the steady-state condition should be considered carefully as well, for example when additional loads on the high side are powered through the bootstrap supply.

7.6 Overview of hard-switching DC-DC converter topologies

In this section, the fundamentals of hard-switching topologies with special emphasis on the resulting diode stress is presented. In particular, the impact of the diode technology on the overall losses of the converter is discussed. Various voltage requirements of DC-DC converter applications influence the usability of different diode technologies. Therefore, one aim of this section is to give guidance in selecting the most suitable diode technology, when considering the different voltage and application requirements.

7.6.1 Principles of hard-switching topologies

Power converters use the switching mode of semiconductors to efficiently convert electrical energy from one form to another. With only minor differences, all converters obey the same principles. In the following section, this fact is utilized to explain the basic principles of hard-switching topologies, and in particular, to describe the operation of diodes in this environment. The basic fundamentals of power diodes used in switch-mode will first be described in detail using the buck-converter which is the most generic topology. Later, these same principles will be applied to other common structures. The particularities of these converter topologies – especially from the diode perspective – will be presented and illustrated.

The schematic representation of a non-isolated asynchronous buck-converter is illustrated in Figure 126. As depicted, it consists of input and output capacitors to stabilize the dc voltages, a power inductor, a power transistor and a power diode. The load, represented as an ohmic resistance, symbolizes that converted electrical energy is transformed into another form of energy, such as mechanical or thermal energy.

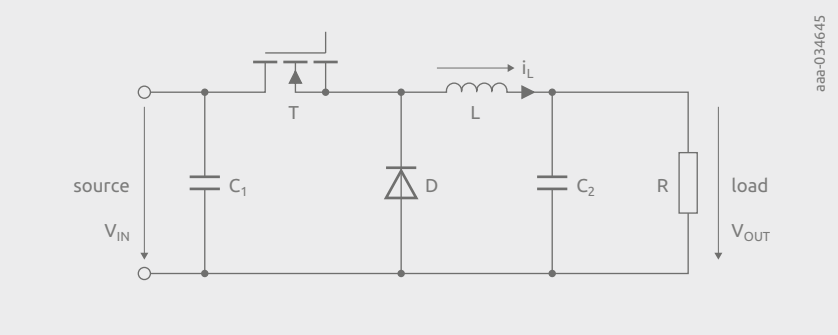

Figure 126 | Schematic of a buck converter.

For the following explanations and waveforms, some assumptions have to be made for the sake of simplicity:

1. All devices are assumed to be ideal:
   - No losses
   - No parasitic elements
   - Ideal switching transitions with infinite steepness
   - Zero on-resistance and cut-in voltage for the power semiconductors
   - Infinite off-resistance for the power semiconductors
   - Passive components have a purely linear behavior
2. The converter operates in steady-state conditions.
3. The capacitors have finite capacitances, but their values are high enough such that variations in their voltages can be ignored.
4. The inductor has a finite inductance and its current can possess a triangular AC ripple current in addition to its DC bias current.
5. A fixed switching frequency is used. The voltage conversion from input to output is controlled via the duty cycle.

Once the principal function of the converter is described and the behavior of power diode has been shown, the non-ideal behavior of the diode in a hard-switching DC-DC converter application will be described in greater detail.

Given the previously-mentioned simplifications, a buck (also called step-down) converter converts an input DC voltage V_{in} into a lower output DC voltage V_{OUT} by periodically switching the transistor T on and off. The current paths during on-state and off-state of the transistor are depicted in Figure 127 and Figure 128. The corresponding, idealized, triangular inductor current waveform for both states is illustrated in Figure 129. During the on-state, energy is stored in the magnetic field of the power inductor, resulting in a linear rising current flowing through it. Once the transistor is turned-off, the stored energy in the magnetic field cannot instantly vanish. As a result, the current flows through a new path presented by the power diode. This operation is called 'free-wheeling' and the diode is often referred to as a 'free-wheeling diode' which maintains the energy supply of the load through the stored energy in the power inductor and output capacitor, resulting in a linearly-declining inductor current and declining stored magnetic energy. In this way, energy is transferred from the input to the power inductor, and stored in its magnetic field during on-state, and this particular amount of energy is then transferred from the magnetic field to the load during freewheeling. This process happens periodically providing a continuous power supply to the load.

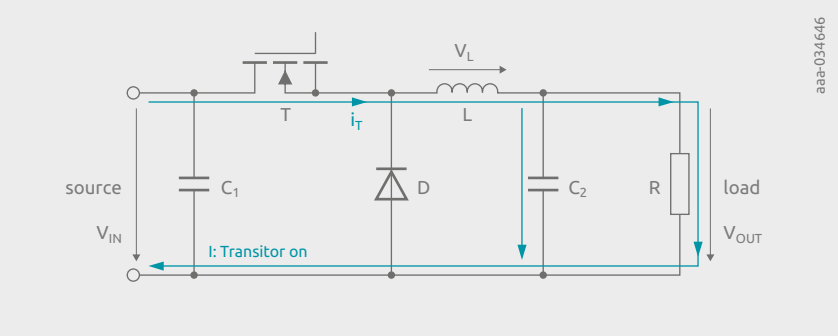

Figure 127 | Transistor in on-state and diode in off-state.

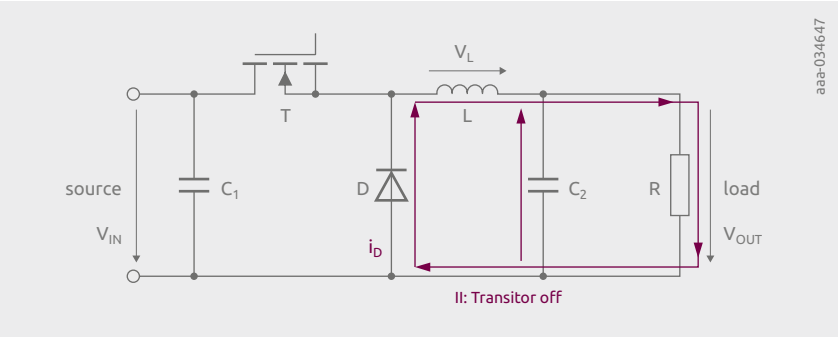

Figure 128 | Transistor in off-state and diode in on-state.

Regardless of the load condition of the converter, and the amount of stored energy in the magnetic field of the power inductor, the waveform always remains triangular, as shown in Figure 129 , but the inductor current may possess zero current phases. Three different operational modes can be distinguished. First, the inductor current can be continuously non-zero during the switching period. Second, the current can reach zero at the exact end of the period. Thirdly, it can reach zero during the freewheeling phase prior to the end of the switching cycle. These three modes are referred to as continuous conduction mode (CCM), boundary conduction mode (BCM), and discontinuous conduction mode (DCM) respectively, as shown in Figure 130.

CCM, BCM and DCM will affect the loss distribution of the diode. These losses will be explained for the buck converter and then for the other common topologies.

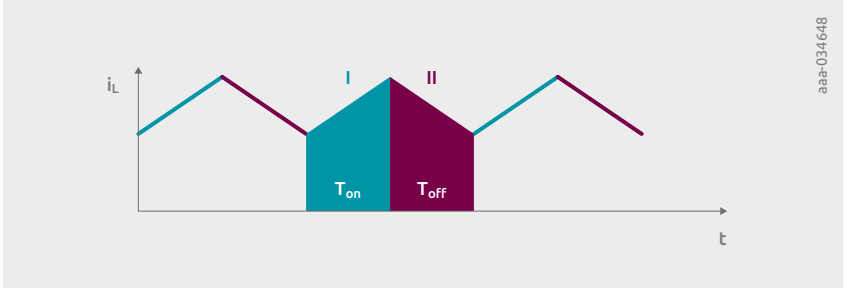

Figure 129 | Inductor, transistor and diode current waveforms.

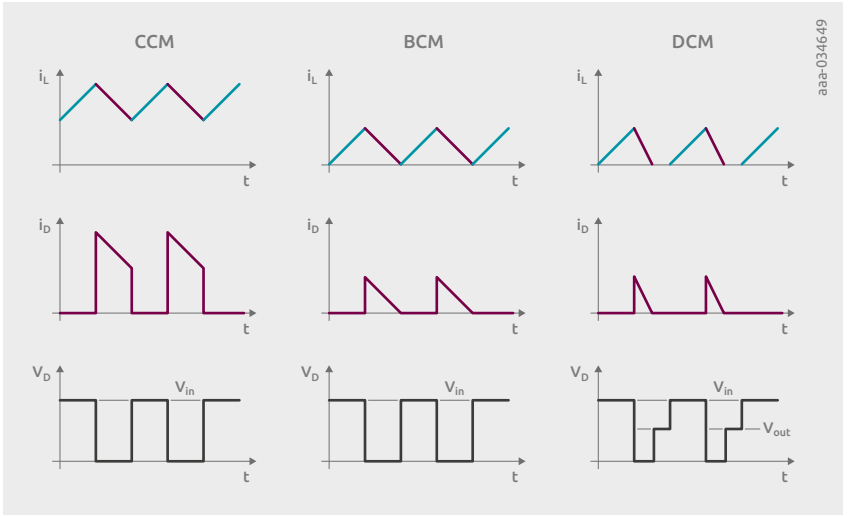

Figure 130 | Diode current and voltage waveforms in a buck converter under continuous current mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM) conditions.

7.6.2 Diode power losses in CCM, BCM and DCM

The depicted triangular current waveform of the inductor assumes lossless components in a buck converter. In reality, a power converter is obviously not lossless. Nevertheless, in the majority of real world designs with lossy inductors, this triangular waveform assumption still holds true. The reason for this is because the amount of stored magnetic energy per cycle is usually magnitudes higher than the energy loss per cycle. Therefore, only a small amount of energy loss is neglected compared to the stored energy in the magnetic field. In real world applications, the true inductor waveform follows an exponential function but appears to be a triangular waveform because the time constant of it is much higher than the switching period of the converter. As a consequence, the loss mechanism in the diode can be described by using the lossless triangular waveforms.

Conduction loss of the diode

Looking at the diode currents in Figure 131, it can be seen that the diode current consists of a DC portion and an AC portion. That means that depending on the I-V-curve (see Figure 132) of the diode, at each moment during the diode conduction phase the instantaneous power losses in the diode are different.

The total conduction losses can be expressed as the mean value of the instantaneous power losses during the converter operation:

$$P_c = \frac{1}{T}\int_0^T P_c(t)\cdot dt = \frac{1}{T}\int_0^T i_d(t)\cdot v_F(id(t),T_j)\cdot dt$$

With T being the duration of one switching period. Usually, the non-linear behavior of the diode's I-V-curve prohibits the solution of this equation. In particular, the feedback of the losses on the junction temperature T_j which in return, affects the I-V-curve of the lossy diode, leads to a complex non-linear equation. Therefore, the complete thermal path from junction to ambient has to be taken into account. The conduction loss equation for P_c has to be solved iteratively, or by using numerical methods or simulation.

However, in order to estimate the losses analytically, the expected worst case conditions should be used for a first initial calculation. That means that besides the full knowledge of the converter operational conditions, the following assumptions are needed:

- Given and fixed worst-case ambient temperature $T_{a(max)}$
- Maximum thermal resistance from junction to ambient
- Worst-case I-V-curves of the chosen diode
- Knowledge of the switching losses and blocking losses of the diode

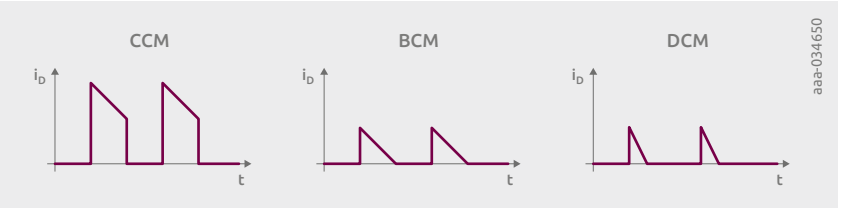

Figure 131 | Diode current waveform in CCM. BCM, DCM.

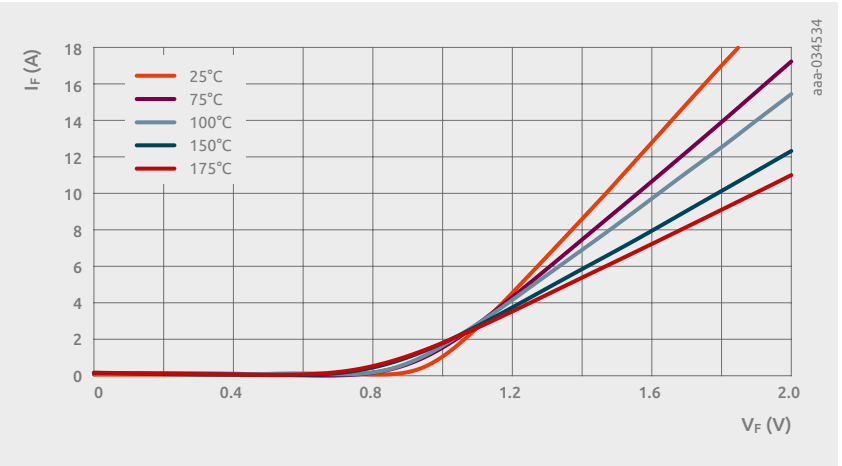

Figure 132 | I-V curve of SiC diode PSC1065K at different junction temperatures.

By simplifying and expressing the corresponding I-V curve characteristics of the diode using a differential resistance r_d and a cut-in voltage V_{F0} an analytical worst-case conduction loss estimation can be performed. With this analysis and the actual triangular DC-biased diode current waveform of the converter, the complex equation of the conduction loss of the diode can be simplified to:

$$P_c = \frac{1}{T}\int_0^T P_c(t)\cdot dt = \frac{1}{T}\int_0^T i_d(t)\cdot v_F(id(t),T_j)\cdot dt \sim V_{F0}(T_j)\times I_{d(avg)} + r_d(T_j) \times (I_{d(rms)})^2$$

Where $I_{d(avg)}$ equals the average value and $I_{d(rms)}$ the root mean square value of the diode waveform.

If this calculated worst-case conduction loss, combined with switching and blocking loss, is less than the maximum power which the device can dissipate through the given thermal resistance, the diode will operate under stable conditions. Moreover, this calculated loss can be used to estimate the corresponding junction temperature which will be lower than the initially assumed worst-case junction temperature. As a next iterative step, and to improve the accuracy of the calculation, the I-V curve corresponding to the calculated junction temperature can be used instead of the worst-case I-V curve. By doing so, the newly calculated conduction losses will be lower and more accurate.

Blocking loss of the diode

This element of the power losses of the diode only occurs during blocking operation. As depicted in Figure 130, during blocking operation, the off-state voltage V_{off} can be assumed to be a constant value. During the blocking phase, the diode is thus permanently reverse-biased with the off state voltage V_{off}. The imperfection of each diode technology during reverse operation causes a small leakage current $i_{leakage}$. The actual magnitude of this leakage current is dependent on the applied negative reverse voltage and the associated junction temperature. As a result, the associated diode leakage current, in combination with the off-state voltage, generates losses. Although the leakage current is comparably small due to the high off-state voltage, the resulting loss can be significant depending on the chosen diode technology. This loss portion is called blocking losses and can be described as:

$$P_b = \frac{1}{T}\int_0^T P_b(t)\cdot dt = \frac{1}{T}\int_0^T V_r \cdot i_{leakage}(V_{off}, T_j)\cdot dt = V_{off} \times i_{leakage}(V_{off}, T_j) \times (1-\delta)$$

With δ being the duty cycle of the converter. As can immediately be seen, the blocking loss equation depends on the off-state voltage during blocking operation, the leakage current as a function of the applied reverse bias V_{off} and the actual junction temperature, as well as the duty cycle of the converter. Thus the equation is non-linear which is caused by the complex non-linear behavior of the leakage current against junction temperature, and the applied off-state voltage. Additionally, the feedback of this loss on the junction temperature, and thus, the thermal path from junction to heatsink, is required. This loss portion can only be accurately calculated by using iterative steps or numerical solution approaches.

In order to estimate the losses, a comparable approach to the conduction loss estimation method can be used. For this, the worst case leakage current is used for the initial calculation. Additionally, the following assumptions are accepted:

- Given and fixed worst-case ambient temperature $T_{a(max)}$
- Maximum thermal resistance from junction to ambient
- Worst-case I-V curves of the used diode
- Knowledge of the switching losses and conduction losses of the diode

By using the worst-case leakage current, which is usually at the highest junction temperature, the associated worst-case blocking loss can be calculated using the above equation. If the device has the capability to dissipate more power through its thermal resistance than the total generated power losses, consisting of the conduction loss, switching loss and calculated worst-case blocking loss, the diode can operate under steady state conditions. Furthermore, the associated junction temperature – given the assumption of worst case leakage current – can be calculated, which can be used for the next iterative calculation. This calculated junction temperature can then be used to determine the actual effective leakage current, which will be lower than the worst case leakage current.

By repeating the blocking loss calculations according to the equation above, and by using the newly-calculated leakage current instead of the worst case leakage current, the calculated blocking loss will be more accurate and also lower than the initial approximation. By successive repetition of this iterative process – the re-calculated blocking losses, corresponding junction temperature, and newly-determined corresponding reverse static characteristics of the diode – the accuracy of this estimation will improve, and the iterative steps will ultimately converge.

In the majority of switched-mode applications where the topology is equipped with silicon PN diodes or SiC diodes, the occurring blocking loss is very low and can usually be neglected in the total power loss calculation. For Si-based Schottky diode technologies, however, the leakage current and the associated blocking losses can become a significant factor, especially for low V_F types (low Schottky barrier); therefore these losses must be taken into account.

Switching loss of the diode

The transition from off-state to on-state of the diode and vice versa is not ideal. In Figure 133, both transition phases, diode turn-on and diode turn-off, as part of the inductor current phases are shown. The phase I→II describes the diode turn-on and phase II→I the diode turn-off. During these transitions, diodes experience a loss which is neither static on-state loss nor static off-state loss.

This loss portion is called switching loss, dynamic loss or recovery loss, and can be distinguished as forward recovery or reverse recovery loss. All elements, even parasitic elements of the commutation cell, as illustrated in Figure 134, contribute to the losses of the diode, but these will not be discussed in for the sake of simplicity.

Please refer to chapter 1 for switching characteristics of different diode technologies.

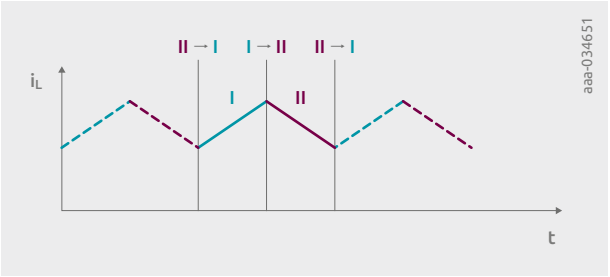

Figure 133
Diode turn-on and turn-off transitions.

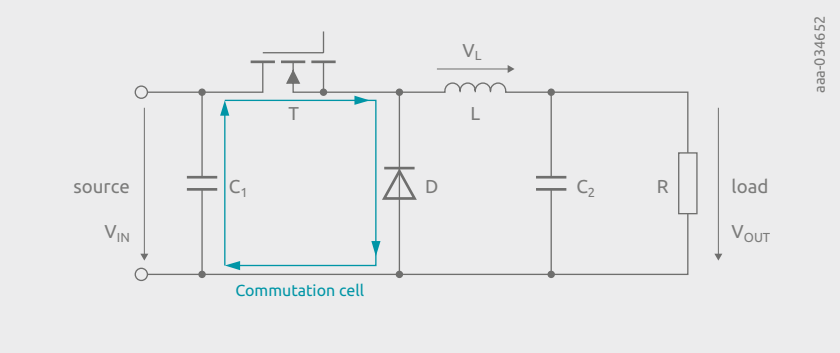

Figure 134 | Commutation, state transition phase.

Forward recovery loss of the diode

Forward recovery occurs during the turn-on transition from an initially reverse biased off-state to the on-state of the diode. After the dv/dt voltage transition, and during the di/dt turn-on ramp, the transient forward voltage drop across the diode is higher compared to the associated static I-V curve. As a result, this transient forward over-voltage causes additional losses beyond the expected losses according to the static I-V curve. It is caused by the initially low conductivity of the diode which takes a finite amount of time to reach its higher final conductivity. The associated forward recovery energy loss can be calculated by integrating the instantaneous power loss, by capturing the diode forward and forward voltage waveforms:

$$E_{on} = \int_{t_0}^{t_0+t_{fr}} i_d(t) \cdot v_F(t,T_j) \cdot dt$$

The integration of the instantaneous energy loss usually covers the period from the start of the di/dt ramp (t0) to when the forward over-voltage collapses back to approximately 110% of the steady-state value (t0+tfr with tfr being the forward recovery time).

The corresponding power loss can be calculated by multiplying the forward recovery energy loss by the switching frequency of the power converter:

$$P_{on} = E_{on} \times f_{sw}$$

The forward recovery characteristic is not a fixed diode-specific behavior; it is influenced by several parameters which, in turn, alter the loss. The amount of over-voltage and thus the amount of forward recovery loss depends on several diode-specific design parameters which will not be discussed in this application-related section. But there are some parameters which are indeed related to the application and influence the forward recovery behavior:

- di/dt slew-rate
- turn-on current (after diode turn-on)
- applied reverse voltage (prior to the turn-on event)
- ambient temperature

However, compared to reverse recovery losses (which are explained in the next section), this loss portion is low and can usually be ignored in the overall total power loss calculation of the diode. Nevertheless, there are some application-specific situations where forward recovery loss can become relevant in hard-switching converter topologies.

In Figure 131, the three different modes of operation are shown. For CCM, both reverse recovery and conduction losses will dominate the loss distribution so that forward recovery is of minor concern. In contrast to the continuous conduction mode, in boundary and discontinuous conduction modes the diode turn-off under zero current conditions will result in a quasi-lossless, reverse-recovery-free turn-off. However, the diode still shows hard turn-on during these operation modes which, in turn, leads to forward recovery loss. A particular situation in BCM and DCM modes where forward recovery may be of relevance for precise power loss calculation is at low-load conditions of the converter combined with high switching frequency and fast slew rates during turn-on.

Reverse recovery loss

In contrast to forward recovery, reverse recovery occurs when the diode has to change from forward conduction state to reverse-biased off-state or blocking state. The turn-off transition happens with a finite di/dt slew rate, as shown in Figure 15 in chapter 1. When, after a certain amount of time (t_2 in Figure 15), the turn-off current reaches zero-crossing, the stored charges, which are still within the diode, prevent the diode from blocking. Instead, the voltage across the diode stays at nearly zero. In order to remove these charges from the device, a significant reverse current flows through the channel. Depending on the chosen diode technology, this charge contains either pure capacitive charge (Schottky), or both capacitive and stored charge due to minority carriers. In case of stored minority carriers in the junction (PN diodes), the time the diode requires to be able to block again is comparably large compared to pure capacitive charge-based devices like Schottky diodes. This is because the stored charge carriers have to recombine in the junction. Please refer to Figure 35 for a comparison between truly capacitive turn-off of a SiC diode versus the bipolar turn-off of a silicon recovery diode.

The associated turn-off energy can be calculated by integrating the instantaneous power within the limits given in Figure 15, with t_2 being the first zero crossing and t_4 being the second zero crossing of the current:

$$E_{off} = \int_{t_2}^{t_4} i_d(t) \cdot v_D(t) \cdot dt - E_c$$

Instantaneous power can be calculated from the captured current and voltage waveforms of the diode. In order not to miscalculate and misinterpret the results, the lossless amount of stored capacitive energy E_c must be subtracted.

An accurate calculation is a complex task and requires many measurements of the reverse recovery waveforms. However, a first rough estimation of the expected losses is given by:

$$E_{off} = Q_{rr} \times V_{r(off)}$$

With Q_{rr} being the specified stored charge in the datasheet and $V_{r(off)}$ the off-state voltage in the application. Although the inductor waveforms are similar for all hard-switching DC-DC-converters, the off-state voltage $V_{r(off)}$ of the diode is stressed differently depending on the chosen technology. Therefore, the following section will describe particularities of widely used converter topologies so that application engineers can consider their loss estimation and diode selection.

7.7 Topologies

In this section, the most common topologies for DC-DC converters are described. All these topologies obey the principles of hard-switching as described in section 6.6.1. Furthermore, the loss calculation is also always similar for all topologies and has already been described in section 6.6.2. Therefore, only the individual particularities of the topology and their impact on losses will be discussed.

7.7.1 Buck converter

A buck converter, also known as a step-down converter, is a system which converts a DC input voltage to a DC output voltage with lower value using the switching mode of power semiconductors. A schematic representation of the non-isolated topology of an asynchronous buck converter is given in Figure 126. As described in the previous section, 6.6.1, and illustrated in Figure 130, the diode has to block the input voltage V_{in} (transient overvoltage excluded). Therefore, for the selection of the diode, the highest expected average and RMS diode current, as well as the highest input voltage must be taken into account for the appropriate current and voltage ratings.

The conduction loss calculation can be used as described in section 6.6.2.1. This calculation is universally true for all converters, so no adaptations are required. On the other hand, the remaining loss portions, blocking loss and forward as well as reverse recovery loss are affected by the topology choice. For blocking loss estimation in a buck converter, the maximum reverse voltage $V_{r,max}$ across the diode equals the maximum DC input voltage $V_{in,max}$. The associated leakage current at this voltage needs to be taken into account. Regarding the forward and reverse recovery losses, measurements at worst-case operating conditions (highest junction temperature, highest expected commutation speed and highest forward current at maximum input voltage) are required to estimate the highest losses the diode will have to handle in the buck converter. If BCM or DCM are the only modes of operation, reverse recovery losses usually can be neglected.

7.7.2 Boost converter

The opposite of a buck converter, the boost converter elevates a lower DC input voltage to a higher DC output voltage. The schematic of the boost converter topology is depicted in Figure 135. In contrast to the buck – and excluding transient over-voltages during diode turn-off transition – the diode has to block and withstand the DC output voltage rather than the DC input voltage (see Figure 136).

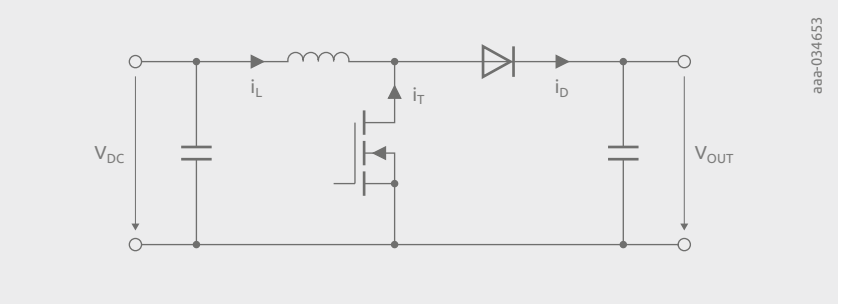

Figure 135 | Schematic of a boost converter

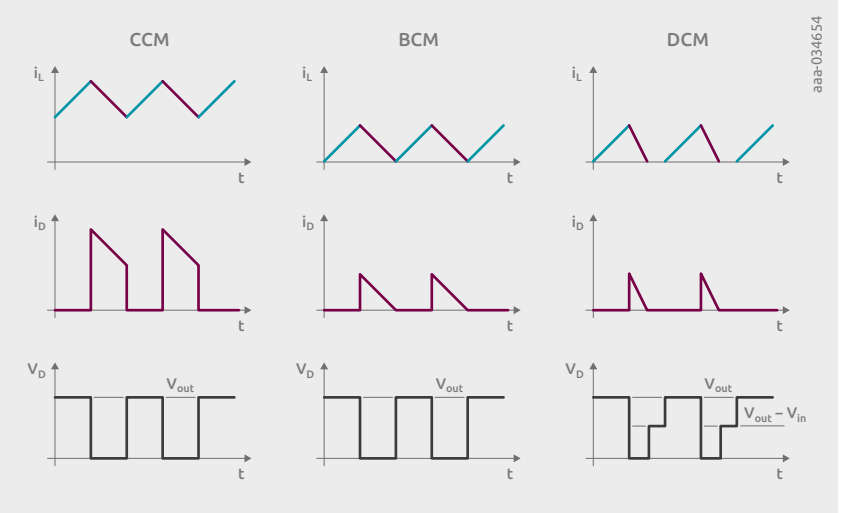

Figure 136 | Diode current and voltage waveforms in a boost converter under continuous current mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM) conditions.

The output voltage related blocking voltage stress must be considered both for the selection of the suitable blocking voltage capability of the diode and also for the power loss calculation.

For the blocking voltage capability, the highest possible voltage conversion rate in the boost converter must be considered for correct diode selection. To calculate the blocking loss, the reverse and forward recovery losses and the maximum output DC voltage (rather than the input voltage) must be used. This is the major difference from a buck converter, especially when assuming a fixed input DC link voltage V_{in}. This means for the maximum reverse voltage $V_{r(max)}$ across the diode, $V_{r(max)} = V_{OUT(max)}$. So, the corresponding diode leakage current at highest output voltage of the converter must be used for accurate blocking loss estimation. That means that, in contrast to the buck converter, the converter operation at the chosen duty cycle and the resulting DC output voltage at a given fixed DC input voltage, has a direct impact on the voltage stress the freewheeling diodes have to withstand.

For the forward and reverse recovery loss calculations, functions such as junction temperature, commutation speed and forward current have the same impact on the recovery losses as in a buck converter. However, the input voltage is not significant for the recovery loss calculation at a given diode forward current. The recovery behavior and losses vary with the resulting DC output voltage, and thus are implicitly dependent on the duty cycle and the mode of converter operation. Especially under CCM conditions, reverse recovery has a major influence on the loss distribution. Otherwise, the losses are almost negligible due to the zero current turn-off transition (zero current switching) of the diode.

7.7.3 Buck-boost converter

The buck-boost converter unifies the properties of both buck and boost converters. Buck-boost is able to convert a input DC voltage to a higher, equal or lower DC output voltage V_{OUT} depending on the chosen duty cycle. The topology of a buck-boost-converter is illustrated in Figure 137.

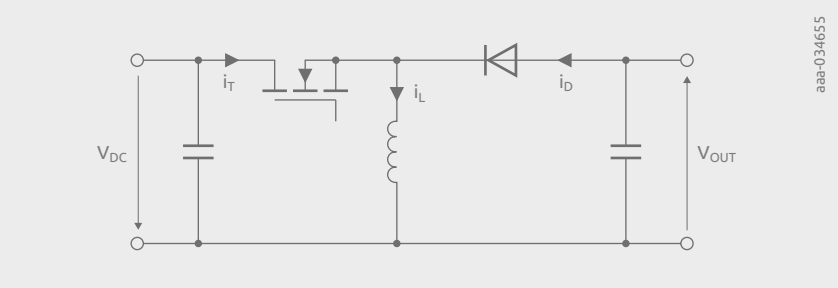

Figure 137 | Schematic of a buck-boost converter.

The buck-boost converter consists of the same number of elements as the buck and boost converters. However, the arrangement is different. As can be seen in Figure 137, the power inductor is positioned in the middle between the power semiconductors. As a result, the corresponding energy transfer leads to an inverted DC output voltage compared to the DC input voltage.

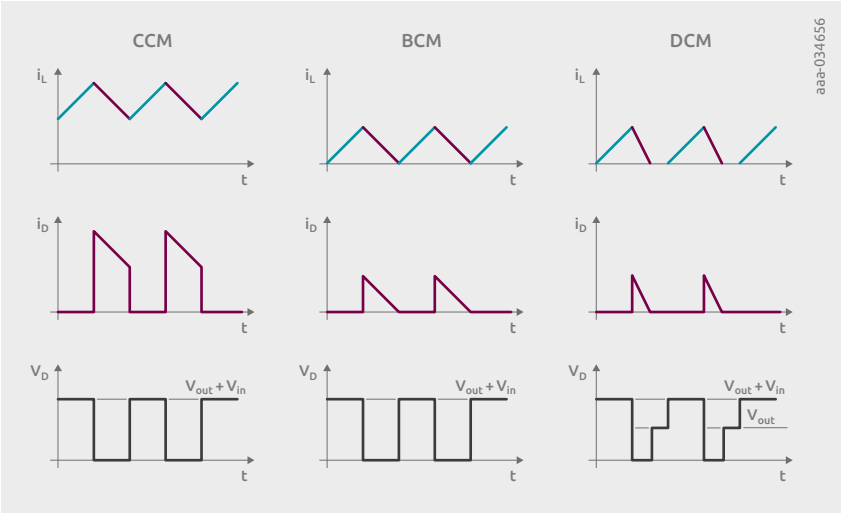

Figure 138 | Diode current and voltage waveforms in a buck-boost converter under continuous current mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM) conditions.

The corresponding current and voltage waveforms of the buck-boost converter are shown in Figure 138. As previously explained, all converters obey the principles of hard-switching which always results in the same triangular waveforms, independent of the actual topology. However, the voltage blocking stress on the diode is topology-dependent. The diode in this particular topology has to block and withstand a voltage, which is the sum of both the DC input and the converted DC output voltages, which is a direct consequence of the inversion behavior of the arrangement. In that regard, the diode losses in a buck-boost converter are affected by both the fixed DC input voltage and the DC output voltage, which is again a consequence of the duty cycle. Therefore the maximum reverse voltage across the diode is: $V_{r(max)} = V_{in(max)} + V_{OUT(max)}$. So the maximum expected output voltage at maximum DC input voltage must be considered for diode selection. Also the recovery losses are dependent on the sum of these two voltages. All other aspects for the recovery loss calculation remain the same.

7.7.4 Flyback converter

A flyback converter is a DC-DC converter whose mode of operation is very similar to the buck-boost converter except that it provides galvanic isolation between the DC input and DC output voltage. The flyback topology can be derived from the buck-boost converter which will not be shown in this publication for sake of simplicity. Galvanic isolation is achieved by using a coupled inductor with two windings which share the same magnetic core, instead of one power inductor. The schematic is shown in Figure 139.

In contrast to a transformer, this coupled inductor principle stores magnetic energy during the transistor turn-on phase. This stored magnetic energy is eventually transferred to the secondary side so that the mode of operation obeys the principles of hard-switching, as previously explained. The turns ratio between primary and secondary side windings provides another opportunity to adjust the DC output voltage at a given DC input voltage, in contrast to previously-mentioned converters. The turn ratio 'a' (here defined as ratio of secondary to primary side winding $\frac{N_s}{N_p}$) also influences the magnitude of the secondary-side current. In all the other previously mentioned converters, the magnitude of current the diode has to carry at the start of the diode phase is equal to the maximum transistor current at the end of the transistor conduction phase (see Figure 129). Depending on the turns ratio 'a', the maximum peak transistor current and diode current may differ. Both secondary and primary sides are coupled via the magnetic flux of the magnetic core so that the primary side and secondary side inductor current are inversely proportional to the turns ratio 'a'. As shown in Figure 140, the secondary side inductor current and the diode current are the same, and the peak value is inversely proportional to the peak transistor and thus peak primary current.

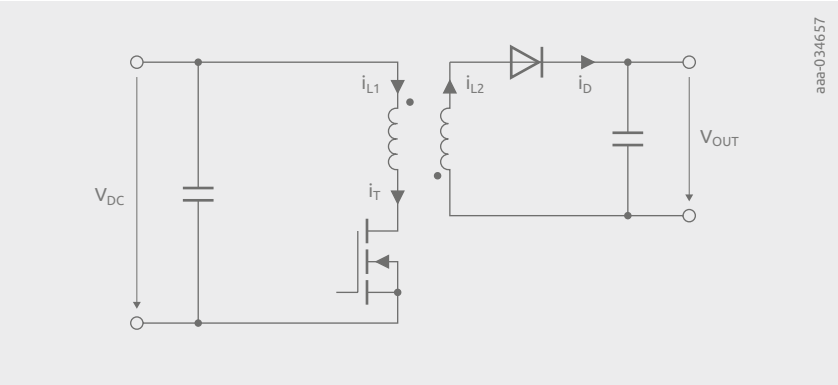

Figure 139 | Schematic of a flyback converter.

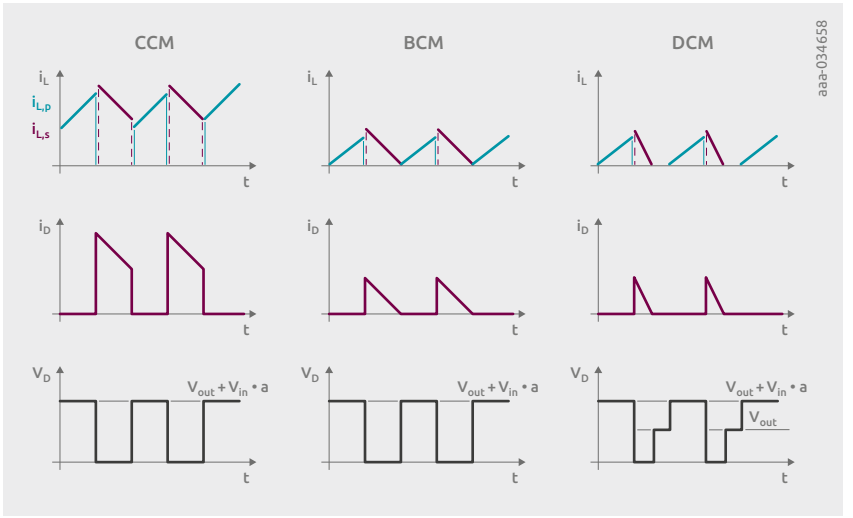

Figure 140 | Diode current and voltage waveforms in a flyback converter under continuous current mode (CCM), boundary conduction mode (BCM) and discontinuous conduction mode (DCM) conditions.

For correct diode selection, another aspect, the turns ratio 'a' of the coupled inductor, must be considered. This affects the blocking voltage capability and also the current rating.

For correct diode selection, another aspect, the turns ratio 'a' of the coupled inductor, must be considered. This affects the blocking voltage capability and also the current rating.

The maximum off-state voltage of the diode excluding transient over-voltages equals the sum of the DC output and the DC input voltage multiplied by the turns ratio. Thus $V_{r(max)} = a \times V_{in(max)} + V_{OUT(max)}$ must be taken into account under all possible converter scenarios (with 'a' being defined as ratio of secondary to primary side winding $\frac{N_s}{N_p}$). The additional dependency of the turns ratio must be considered for blocking and recovery losses dependent on the chosen mode of operation (CCM, BCM DCM). The diode current, on the other hand, is inversely proportional to the turns ratio 'a'. That means that, especially at a low turns ratio, the secondary side inductor current and thus the diode current can be significantly higher. This must also be considered for the conduction loss estimation and diode selection for the chosen diode technology.

Chapter 8
Summary

Discrete diodes are still a very important and basic component of electronic systems. Their electrical and thermal properties as well as their reliability are decisive for the overall performance and robustness of the entire electronic system.

There are a wide variety of diode technologies available in different packages and form factors. This handbook summarizes the choices available on the market and discusses their device structure. Interestingly, there are still new developments in discrete diodes. Specifically, the SiGe diode technology newly developed by Nexperia should be noted here.

The normalization of the currents with respect to the die size in this handbook allows a fair comparison of the different technologies. Both the static and dynamic behavior of the diodes are discussed and compared.

A separate section is devoted to the novel Schottky diodes based on silicon carbide, and the advantages that SiC diodes bring are presented and compared to silicon diodes.

Diode packaging plays no less a role than the semiconductor element housed inside the packaging. Therefore, different package styles for discrete diodes are presented. The associated thermal properties of the diodes are discussed in a separate chapter. Of particular note here is the phenomenon of diode called thermal runaway, which is often overlooked by design engineers and can lead to failures of the system.

Since diodes are also used in critical infrastructure and automotive electronics, the stress tests performed by Nexperia to qualify and release diodes are also touched upon in a chapter in this book.

Last but not least, the last chapter of the handbook discusses important diode applications. Here, the general consideration of losses in switched-mode converters should be emphasized.

For questions and suggestions do not hesitate to contact us.

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Abbreviations

AC	Autoclave
BCM	Boundary conduction mode
CCM	Continuous current mode
C_d	Diode parasitic capacitance
DCM	Discontinuous conduction mode
di/dt	Current edge steepness/slope gradient
D_n	Diffusion coefficient
EFR	Early failure rate
E_{off}	Turn-off energy
E_{on}	Forward recovery energy loss
f_{sw}	Switching frequency
H3TRB	High humidity/high temperature reverse bias
HAST	Highly accelerated stress test–biased
HTOL	High temperature operating life
HTRB	High Temperature reverse bias
i_{boot}	Current through the bootstrap diode
$\hat{i}_{boot}$	Peak current through the bootstrap diode
I_F	Forward current
$I_{F(AV)}$	Average forward current
IFR	Intrinsic failure rate
I_{FRM}	Repetitive peak forward current
I_{FSM}	Non-repetitive peak forward current
IOL	Intermittent operational life
I_R	Reverse current
I_{RM}	Peak reverse recovery current
I_{RMS}	Root mean square of forward current
I_Z	Zener current
J_R	Reverse current density
MPS	Merged PIN Schottky
MSL	Moisture sensitivity level
n_i	Intrinsic carrier concentration
N_p	Primary side winding
N_s	Secondary side winding
P_B	Blocking loss
P_C	Conduction loss
P_{diss}	Dissipated power
$P_{generated}$	Self-heating generated by reverse leakage current
P_{load}	DC conduction loss
P_{on}	Forward recovery loss
$P_{R(AV)}$	Average reverse power dissipation
P_{tot}	Total power dissipation
q	Elementary charge
Q_{rr}	Reverse recovery charge

r_{dif}	Differential resistance
R_T	Normalized thermal resistance is with respect to package footprint
$R_{th(j-a)}$	Thermal resistance junction to ambient
$R_{th(j-c)}$	Thermal resistance junction to case
$R_{th(j-mb)}$	Thermal resistance junction to mounting base
$R_{th(j-sp)}$	Thermal resistance junction to solder point (usually the cathode path)
$R_{th(j-top)}$	Thermal resistance junction to top
$R_{th(sp-a)}$	Thermal resistance solder point to ambient
SF_{rr}	Softness factor
SiC	Silicon carbide
SiGe	Silicon germanium
SOA	Safe operating area
S_Z	Thermal coefficient of Zener voltage
T_{amb}	Ambient temperature
T_c	Case temperature
TC	Temperature cycling
T_j	Junction temperature
T_{jmax}	Specified maximum junction temperature
t_p	Pulse width
t_{rr}	Reverse recovery time
TS	Temperature shock
T_{stg}	Storage temperture
UHAST	Highly accelerated stress test
V_{Cboot}	High-side supply voltage–voltage across bootstrap capacitance
V_{drift}	Forward voltage drop across drift layer
V_f	Forward voltage drop
V_{FRM}	Peak forward recovery voltage
V_{ms}	Forward voltage drop across metal semiconductor interface
V_{pn}	Forward voltage drop across pn junction
V_R	Reverse voltage
V_Z	Zener voltage
$Y_{th(j-top)}$	Thermal coefficient junction to top
$Z_{th(x-y)}$	Thermal impedance between point x and y
δ	Duty cycle
ΦB	Barrier height

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